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FLMS0

DIS M/B Schematic Document

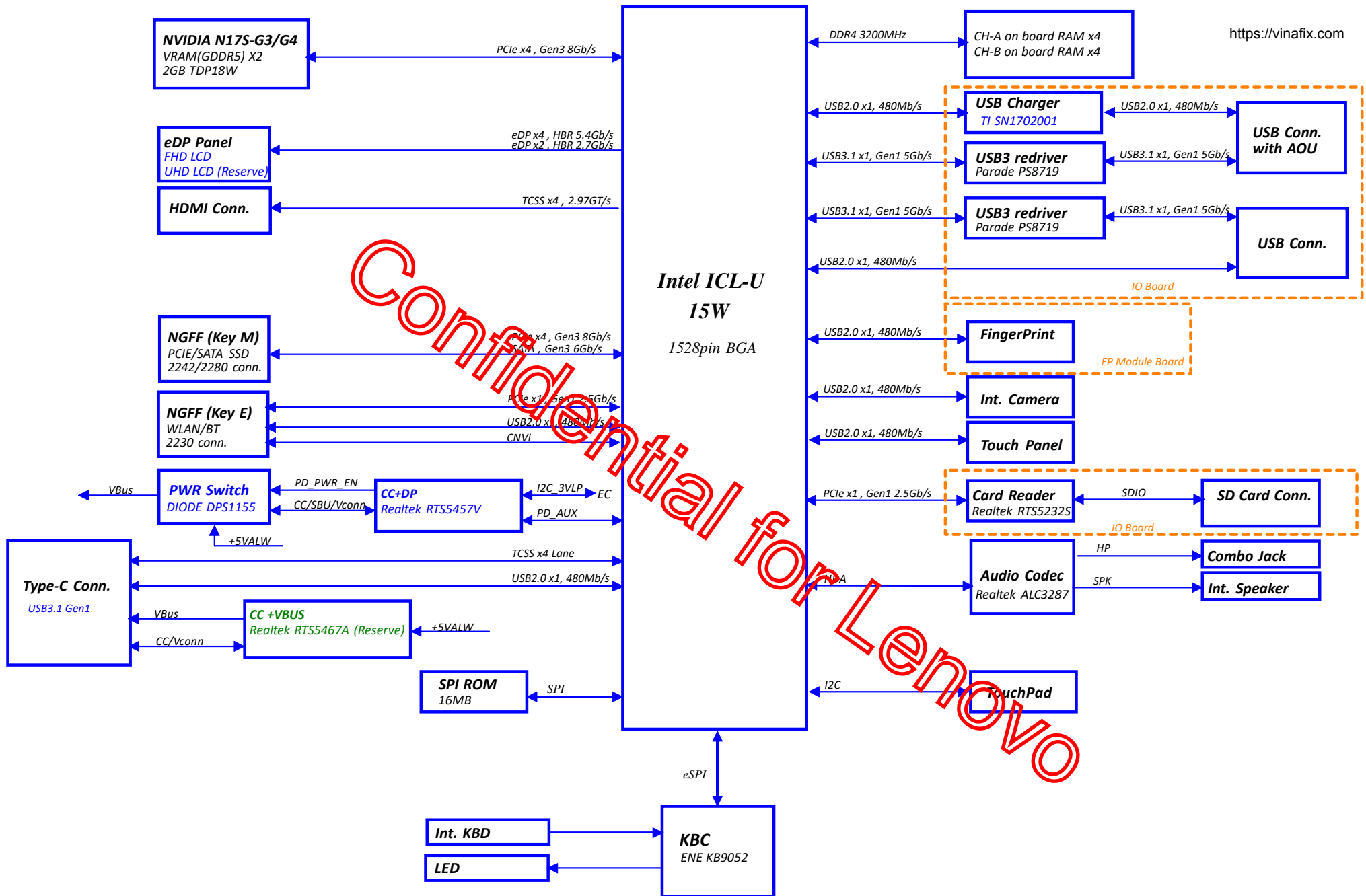
Intel Ice Lake-U Processor with DDR4 Memory Down

2019-08-22

LA-J551P

REV : 0 . 2

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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<https://vinafix.com>

power plane State				
	+12.6VB	+5VALW +3VALW +1.8VALW	+1.2V +2.5V	+5VS +3VS +1.8VS +0.6VS +1.05V_VCCST +1.05VS_VCCSTG +VCCIN +VCCIN_AUX +1.8VS_DGPFU +1.8VS_DGPFU_AON +VGA_CORE +1.0VS_DGPFU +1.35VS_VRAM
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Item	BOM Structure
GPU N17S-G0/G2	DISE@ UMA@
Debug	DCI@ SDP@
Memory Down - SDP Package	SDP_CHB@
Memory Down - DDP Package	DDP@ DDP_CHB@
Only CHB Memory Down	CHB@
Intel CNVi	CNVi@
Keyboard BackLight	KBL@
EMI Category	EMT@
ESD Category	ESP@
RF Category	RFP@
Normal FP Device	FPE@
SLIM_FP	SLIM_FP@
+12V FAN CAP	
+5V FAN CAP	
CPU MIC (Reserve)	Aarray_MIC@ Single_MIC@ SOIX@ NOSOIX@
Modern standby	
Product select	
DDP/Memory Down CHB	CHB@
GPU G6 Mode	GCE@
Touch Sensor Board	NOGC6@
TSP	TS@
EC9052G_Capsules	EC9052_c@
Option Bypass USB Charging	SON_AOU@
RMT tool test	RMT@
	QSG@_R@ QSPP_R@ QSQV_R@ QSVH_R@ QQSN_R@
CPU select	

Item	BOM Structure
DGPU chip select	N17S_G0_R1@
	N17S_G0_R3@
	N17S_G2_R1@
	N17S_G2_R3@
VRAM chip select	VRAM_M2G_R1@
	VRAM_M2G_R3@
	VRAM_H2G_R1@
	VRAM_H2G_R3@
	VRAM_S2G_R1@
	VRAM_S2G_R3@

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	Touch Screen
5	
6	Camera
7	Fingrt Print
8	
9	
10	NGFF WLAN+BT

[illegible]

Port	
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	
4	
5	
6	

Port	Lane	
1		
2		
3		
4	0	
5	0	
6	1	GPU
7	2	
8	3	
9	1	
10	0	CardReader
11		NGFF WLAN+BT
12	0	
13	3	
14	2	SSD
15	1	
16	0	

Port	
0	
1A	
1B	SSD

Device	Address	Device	Address
Smart Battery	0001_011x_16h	Thermal Sensor (F75305M)	1001_101xb_9Ah
Charger (ISL88739A)	0001_001x_12h	Thermal Sensor (F75397M)	1001_100xb_98h

Device	Address	Device	Address
DDR JDIMM1	1010 010x A4h	Internal thermal sensor	1001 111x 9Eh

	SOURCE	SOC	BATT	CHARGER	KB9052	SODIMM	Thermal Sensor	DGPU
EC_SMB_CK1 EC_SMB_DA1	KB9052 +3VL	X	V	V	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	KB9052 +3VS	X	X	X	X	X	+3VS	+3VS
EC_SMB_CK4 EC_SMB_DA4	KB9052 +3VS	X	X	X	X	X	X	X
SOC_SMBCLK SOC_SMBDATA	SOC +3VS	X	X	X	X	+3VS	X	X
SOC_SML0CLK SOC_SML0DATA	SOC +3VS	X	X	X	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VAL#	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Diagram illustrating three types of USB cables and their corresponding devices:

- ZZZ11** X76_H0G@
X76_HYNYX 2GB
X76H4536L11
- ZZZ12** X76_S2G@
X76_SAMSUNG 2GB
X76H4536L12
- ZZZ13** X76_M2G@
X76_MICRON 2GB
X76H4536L13

UC1 QSQS_R1@ UC1 QSQP_R1@ UC1 QSQV_R1@ UC1 QSQV_R1@ UC1 QSQW_R1@

I7-1065G7 I7-1065G7 I7-1035G1 I3-1005G1 I3-1005G1

SA0000CTB10 SA0000CTB10 SA0000CVQ11 SA0000CVQ11 SA0000CTD10

R1 ☐ UV1 SA0000CC940 ☐ UV2 SA0000CCB30
N17S_G0_R1@ N17S_G2_R1@
N17S-G0 N17S-G2

R3 ☐ UV1 SA0000CC910 ☐ UV1 SA0000CC810
N17S_G0_R3@ N17S_G2_R3@
N17S-G0 N17S-G2

[illegible]

<u>ZZ10</u>	W76_M4G_1CH_3200@	<u>ZZ16</u>	W76_M4G_1CH_2666@	<u>ZZ22</u>	W76_S4G_1CH_2666@
X76 MICRON 4GB SINGEL X76B4839L10		X76 HYNIX 4GB SINGEL X76H4839L04		X76 SAMSUNG 4GB SINGEL X76B4839L02	
<u>ZZ9</u>	X76_M8G_2CH_3200@	<u>ZZ15</u>	W76_M8G_2CH_2666@	<u>ZZ21</u>	W76_S8G_2CH_2666@
X76 MICRON 8GB DUAL X76B4839L09		X76 HYNIX 8GB DUAL X76H4839L03		X76 SAMSUNG 8GB DUAL X76B4839L01	

ZZZ



PCB FL535 LA-H105P
DA6001LE000

X4E

ZZZ14 X4E_D16@

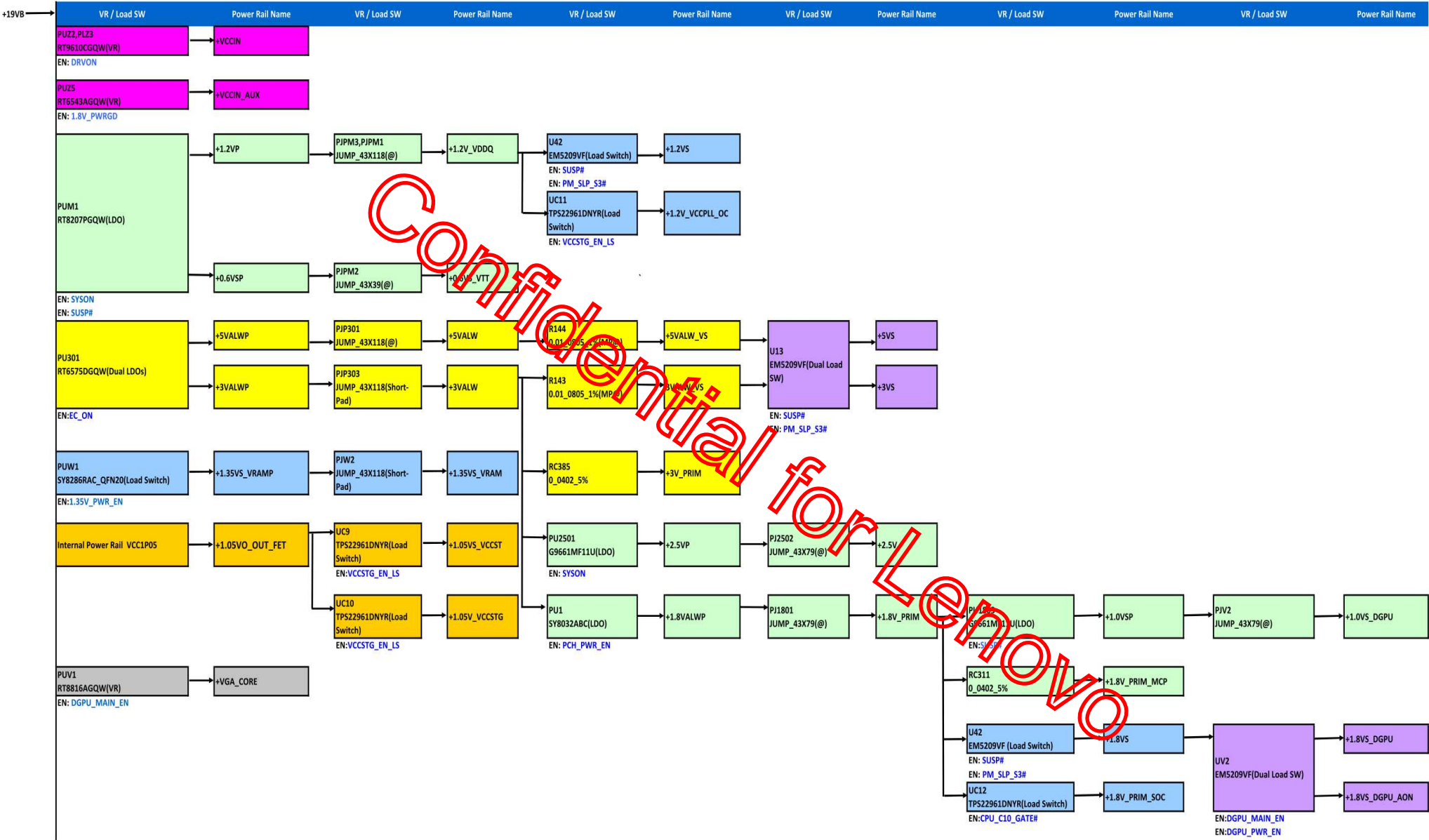


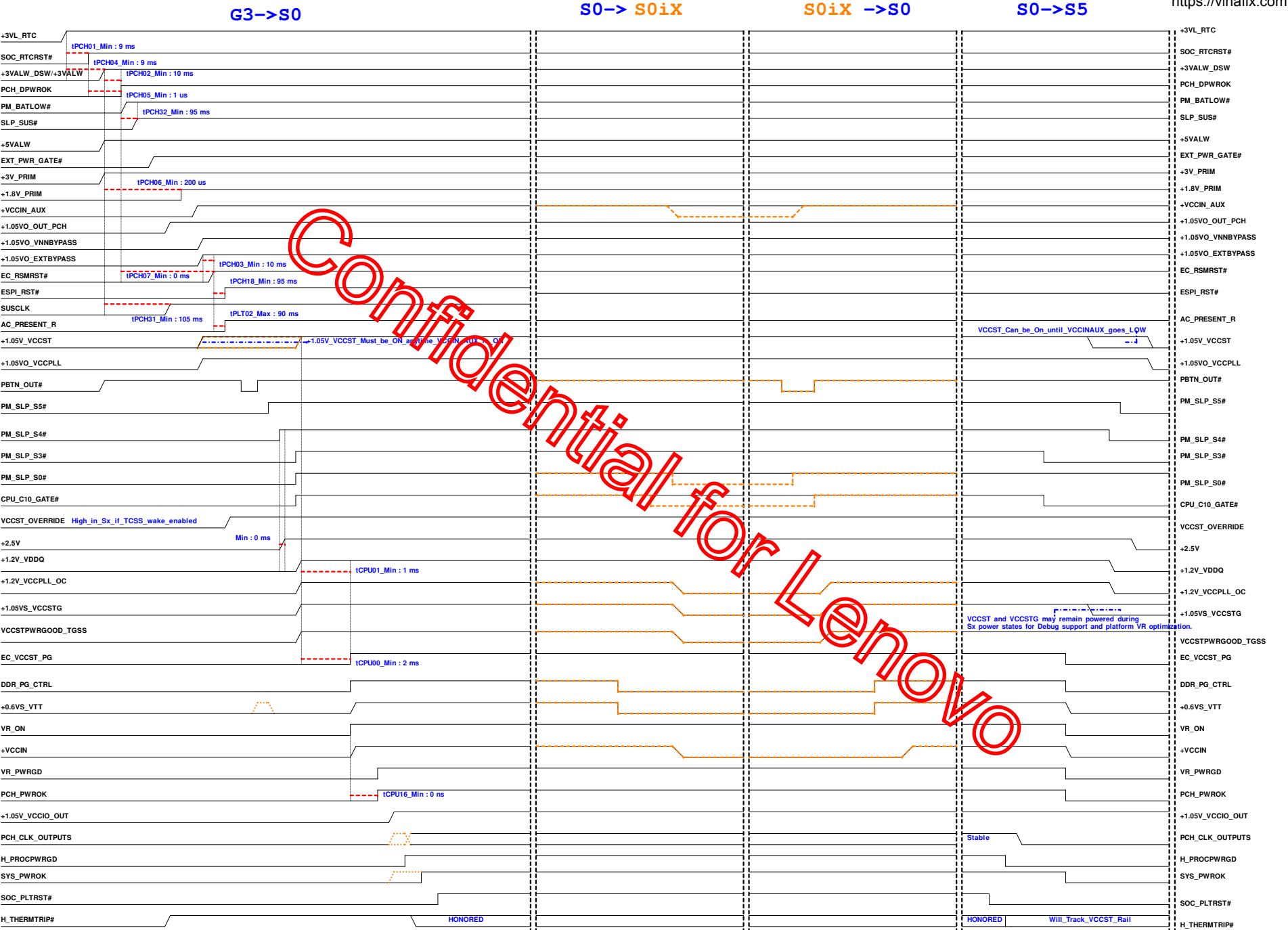
X4E S550- ICL DIS

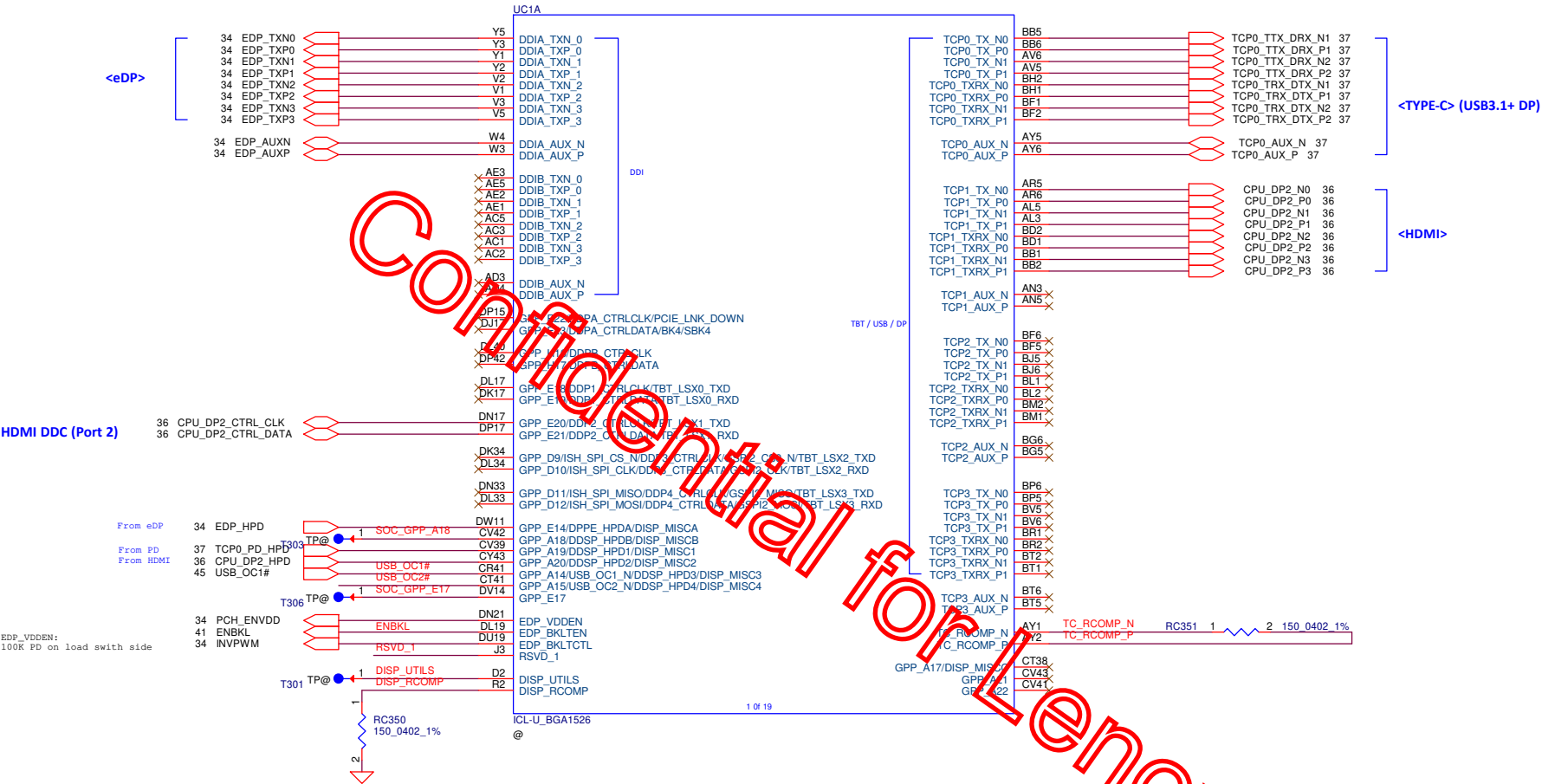
ZZZ15 X4E_UMA@



X4E S550- ICL UMA







RSVD_1:
Follow 573129_ICL_U_DDR4_SODIMM_HW_SCH_RN

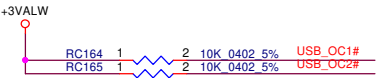
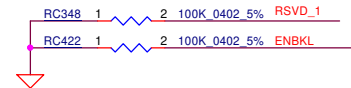
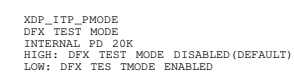
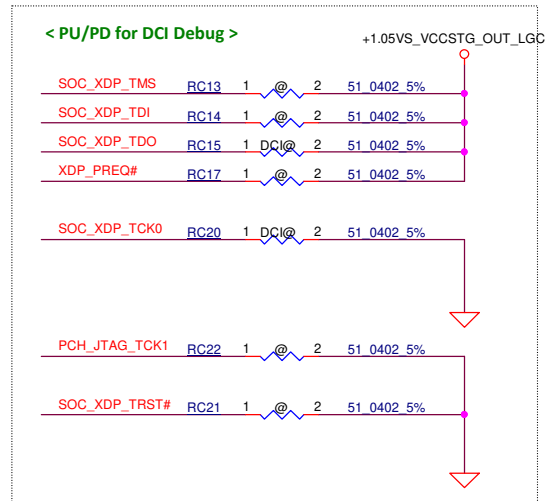
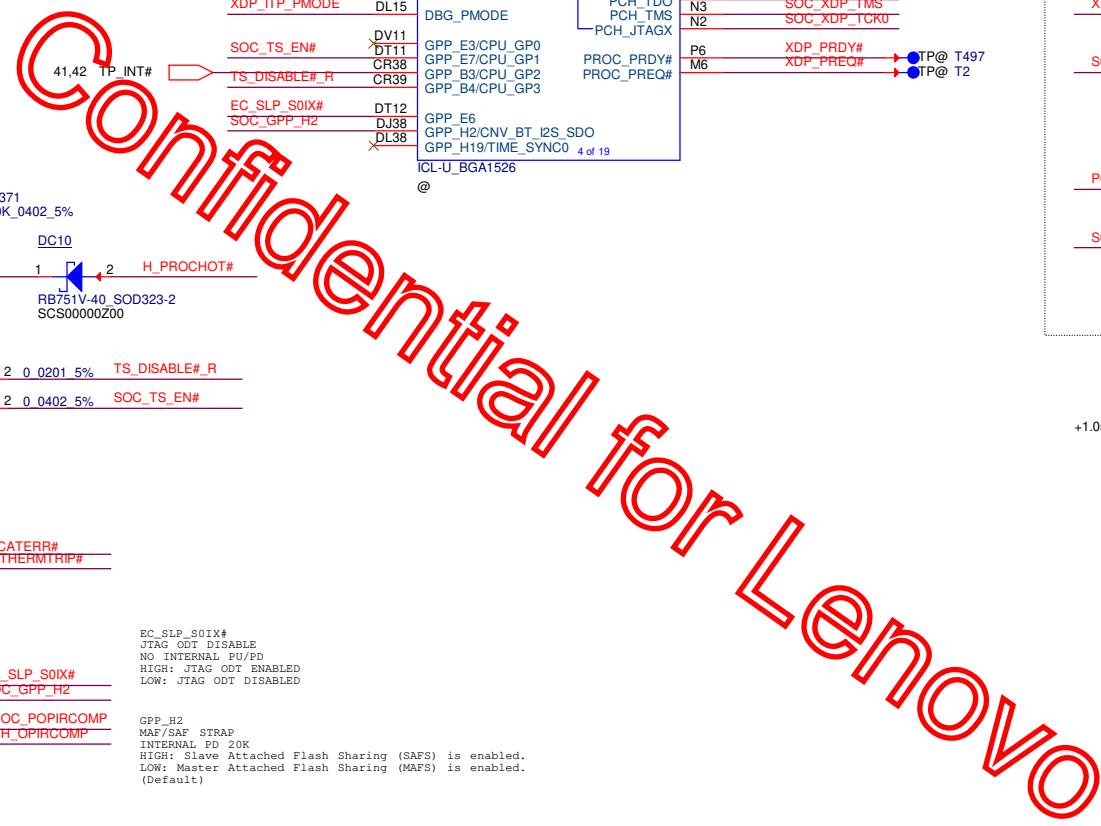


Table 5-11. USB3/USB2 Pin Pairings for USB Type-C Connectors

	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#		2	3	4
PCH USB2 port#	2	3	4	6

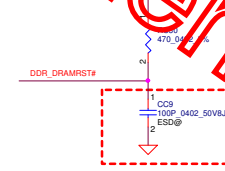
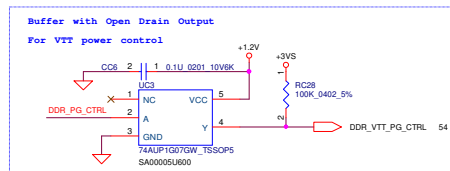
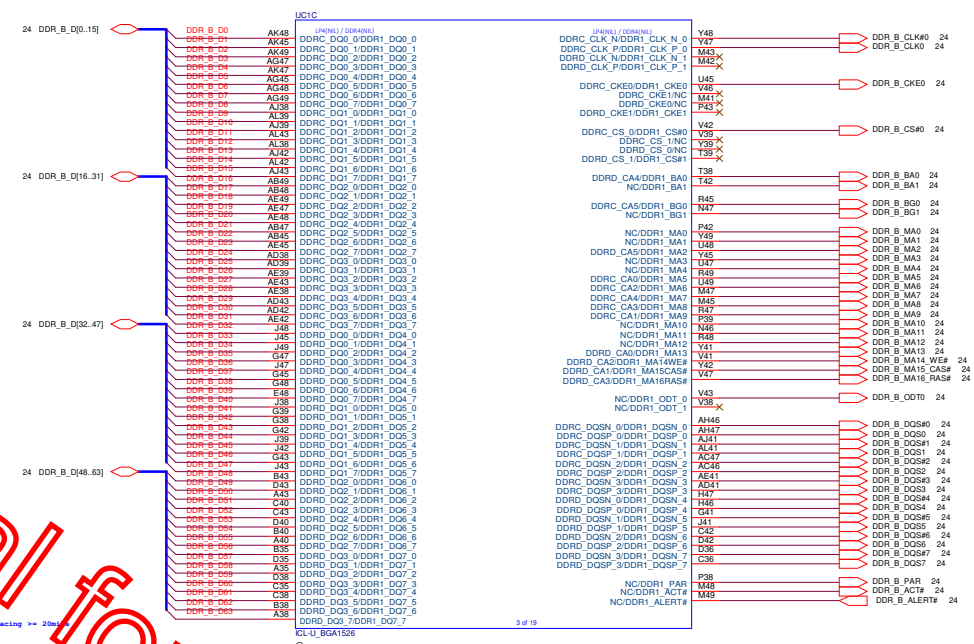
To make split xDCI controller working functionally for different USB-C connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C connectors, but it is not strictly required.

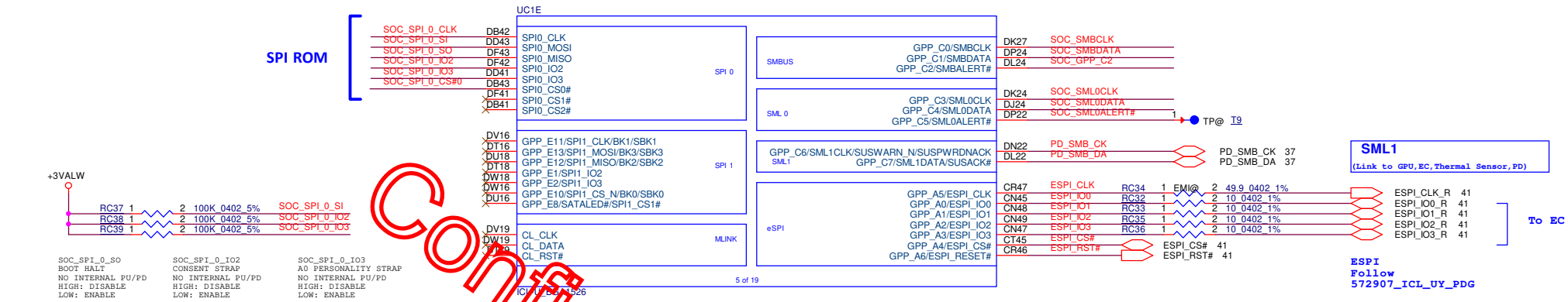


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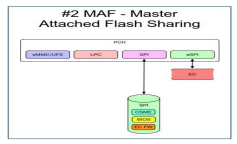
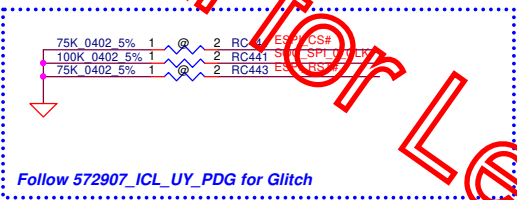
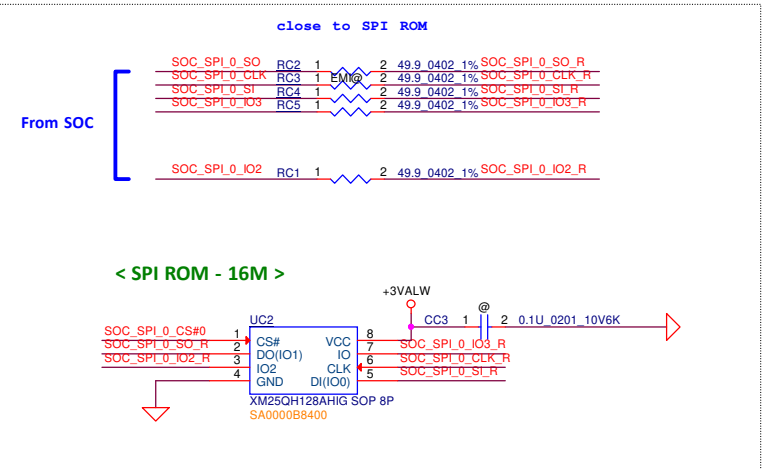
Attention

Pin	Function	Pin	Function
100_0402_1_2	1-RCS	SM ROMCP0	D47
100_0402_1_3	1-RCS	SM ROMCP1	E46
100_0402_1_4	1-RCS	SM ROMCP2	C47
100_0402_1_5	1-RCS	SM ROMCP3	D47
100_0402_1_6	1-RCS	SM ROMCP4	E46
100_0402_1_7	1-RCS	SM ROMCP5	C47
100_0402_1_8	1-RCS	SM ROMCP6	D47
100_0402_1_9	1-RCS	SM ROMCP7	E46
100_0402_1_10	1-RCS	SM ROMCP8	C47
100_0402_1_11	1-RCS	SM ROMCP9	D47
100_0402_1_12	1-RCS	SM ROMCP10	E46
100_0402_1_13	1-RCS	SM ROMCP11	C47
100_0402_1_14	1-RCS	SM ROMCP12	D47
100_0402_1_15	1-RCS	SM ROMCP13	E46
100_0402_1_16	1-RCS	SM ROMCP14	C47
100_0402_1_17	1-RCS	SM ROMCP15	D47
100_0402_1_18	1-RCS	SM ROMCP16	E46
100_0402_1_19	1-RCS	SM ROMCP17	C47
100_0402_1_20	1-RCS	SM ROMCP18	D47
100_0402_1_21	1-RCS	SM ROMCP19	E46
100_0402_1_22	1-RCS	SM ROMCP20	C47
100_0402_1_23	1-RCS	SM ROMCP21	D47
100_0402_1_24	1-RCS	SM ROMCP22	E46
100_0402_1_25	1-RCS	SM ROMCP23	C47
100_0402_1_26	1-RCS	SM ROMCP24	D47
100_0402_1_27	1-RCS	SM ROMCP25	E46
100_0402_1_28	1-RCS	SM ROMCP26	C47
100_0402_1_29	1-RCS	SM ROMCP27	D47
100_0402_1_30	1-RCS	SM ROMCP28	E46
100_0402_1_31	1-RCS	SM ROMCP29	C47
100_0402_1_32	1-RCS	SM ROMCP30	D47
100_0402_1_33	1-RCS	SM ROMCP31	E46
100_0402_1_34	1-RCS	SM ROMCP32	C47
100_0402_1_35	1-RCS	SM ROMCP33	D47
100_0402_1_36	1-RCS	SM ROMCP34	E46
100_0402_1_37	1-RCS	SM ROMCP35	C47
100_0402_1_38	1-RCS	SM ROMCP36	D47
100_0402_1_39	1-RCS	SM ROMCP37	E46
100_0402_1_40	1-RCS	SM ROMCP38	C47
100_0402_1_41	1-RCS	SM ROMCP39	D47
100_0402_1_42	1-RCS	SM ROMCP40	E46
100_0402_1_43	1-RCS	SM ROMCP41	C47
100_0402_1_44	1-RCS	SM ROMCP42	D47
100_0402_1_45	1-RCS	SM ROMCP43	E46
100_0402_1_46	1-RCS	SM ROMCP44	C47
100_0402_1_47	1-RCS	SM ROMCP45	D47
100_0402_1_48	1-RCS	SM ROMCP46	E46
100_0402_1_49	1-RCS	SM ROMCP47	C47
100_0402_1_50	1-RCS	SM ROMCP48	D47
100_0402_1_51	1-RCS	SM ROMCP49	E46
100_0402_1_52	1-RCS	SM ROMCP50	C47
100_0402_1_53	1-RCS	SM ROMCP51	D47
100_0402_1_54	1-RCS	SM ROMCP52	E46
100_0402_1_55	1-RCS	SM ROMCP53	C47
100_0402_1_56	1-RCS	SM ROMCP54	D47
100_0402_1_57	1-RCS	SM ROMCP55	E46
100_0402_1_58	1-RCS	SM ROMCP56	C47
100_0402_1_59	1-RCS	SM ROMCP57	D47
100_0402_1_60	1-RCS	SM ROMCP58	E46
100_0402_1_61	1-RCS	SM ROMCP59	C47
100_0402_1_62	1-RCS	SM ROMCP60	D47
100_0402_1_63	1-RCS	SM ROMCP61	E46
100_0402_1_64	1-RCS	SM ROMCP62	C47
100_0402_1_65	1-RCS	SM ROMCP63	D47
100_0402_1_66	1-RCS	SM ROMCP64	E46
100_0402_1_67	1-RCS	SM ROMCP65	C47
100_0402_1_68	1-RCS	SM ROMCP66	D47
100_0402_1_69	1-RCS	SM ROMCP67	E46
100_0402_1_70	1-RCS	SM ROMCP68	C47
100_0402_1_71	1-RCS	SM ROMCP69	D47
100_0402_1_72	1-RCS	SM ROMCP70	E46
100_0402_1_73	1-RCS	SM ROMCP71	C47
100_0402_1_74	1-RCS	SM ROMCP72	D47
100_0			

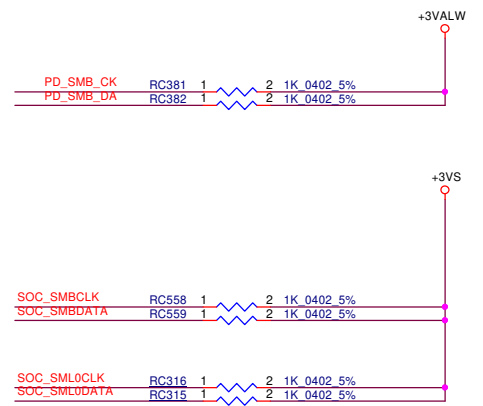




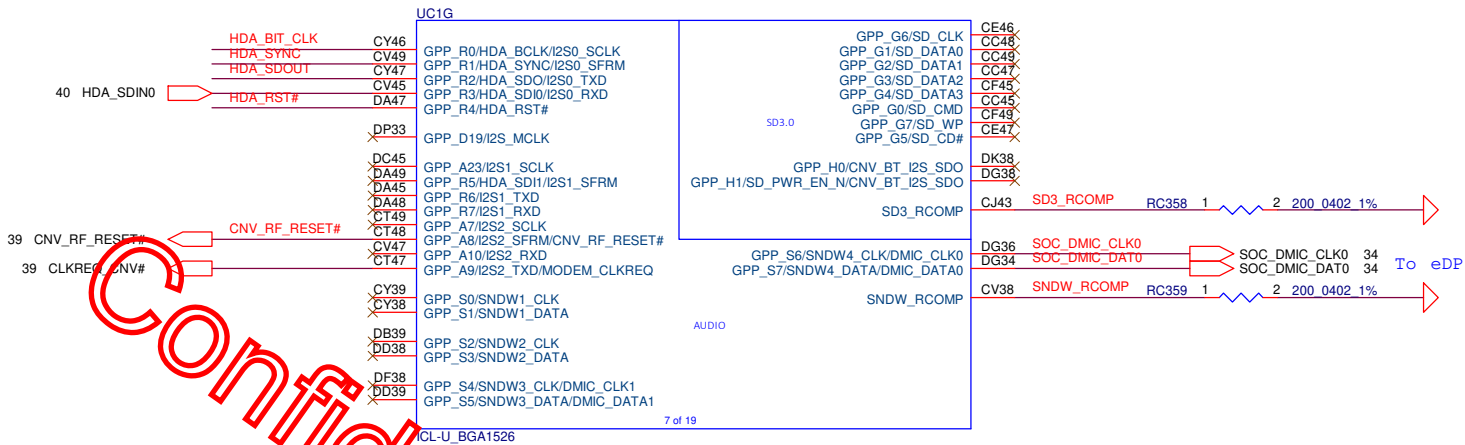
SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



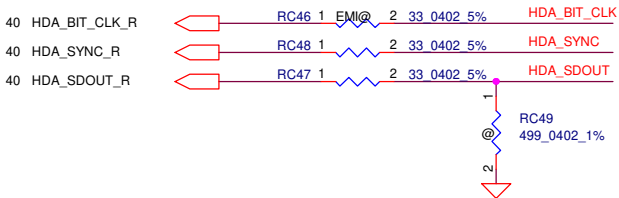
#2 MAF - Master Attached Flash
Single SPI Flash attached to SPI Bus
EC FW access through eSPI Bus



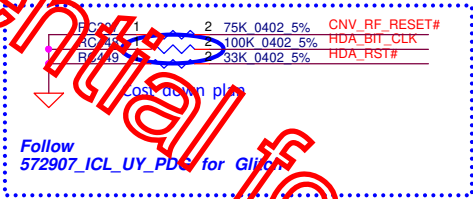
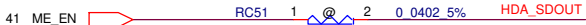
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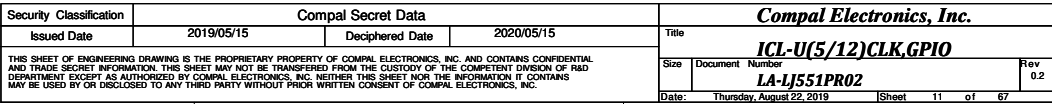
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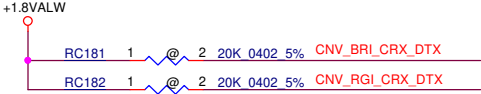
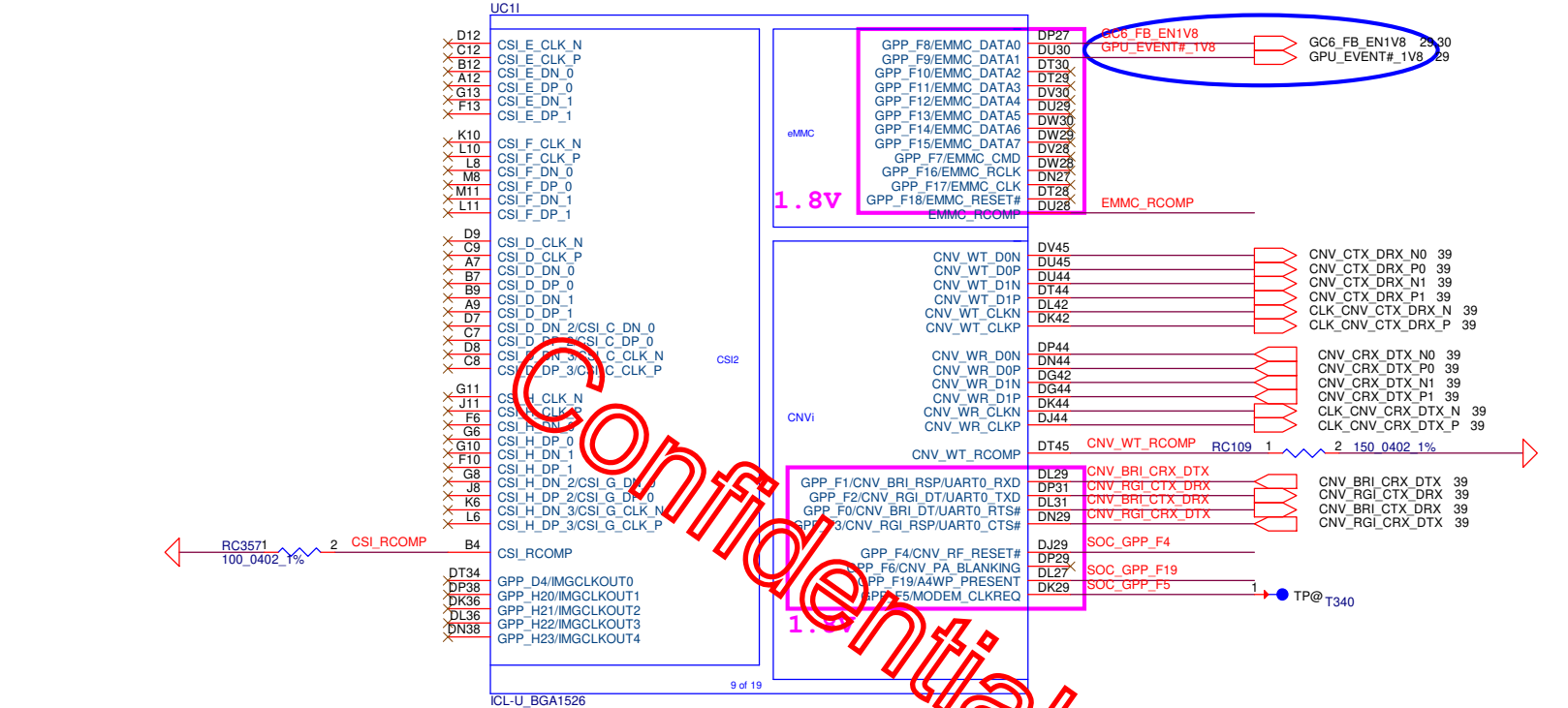


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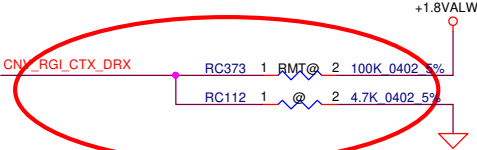
Follow check list reserve

CNV_RGI_CTX_DRX (M.2 CNVi MODES)

0 = Integrated CNVi enable.
1 = Integrated CNVi disable.

NO INTERNAL PU/PD

MLAN side has PU,
just reserve PU on CPU side for RMT test ?

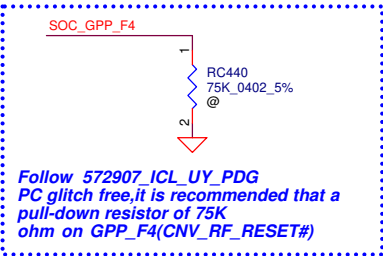
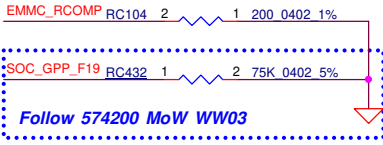
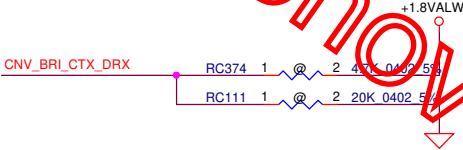


CNV_BRI_CTX_DRX (XTAL SEL)

0 = 38.4/19.2MHZ (DEFAULT)
1 = 24MHZ (25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

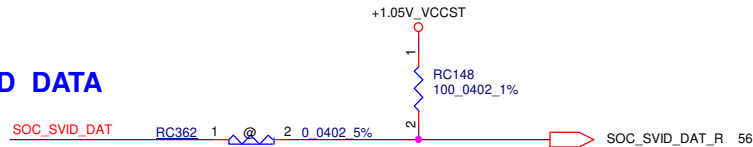
WEAK INTERNAL PU/PD

whether can remove?
this pin have internal

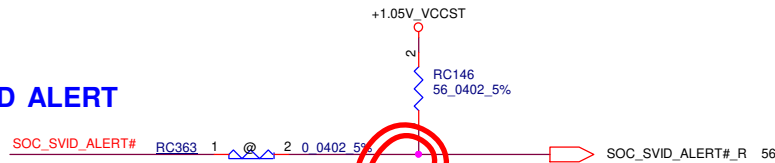


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SVID DATA



SVID ALERT



SVID CLOCK



5.5.10 SVID Topology

Figure 5-54. Routing Illustration for SVID Topology

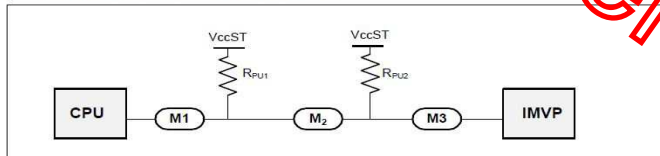
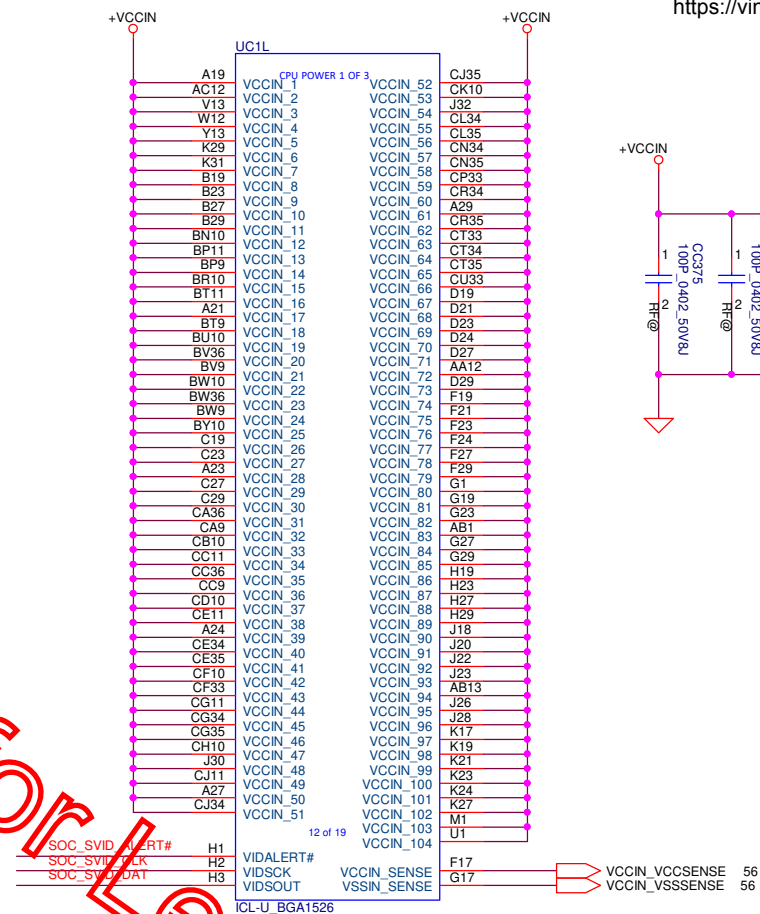


Figure above demonstrates Routing Illustration for SVID Topology, each trace from CPU to VR represents 3 signals: VIDSOUT, VIDSCK, VIDSALERT#.

Table 5-75. SVID Routing Guidelines

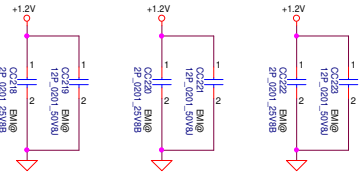
Segment	Tline Type	Reference	Via Count	Max Length, mm	
				Segment	Total
M1	MS/SL/DSL	VSS		75	530
M2	MS/SL/DSL	VSS		380	
M3	MS/SL/DSL	VSS		75	
Topology Guidelines					
SVID Signals		VIDSOUT, VIDSCK, VIDSALERT#			
VIDSOUT platform resistors		Rpu1=100Ω, Rpu2=100Ω			
VIDSCK platform resistors		Rpu1=Empty, Rpu2=45Ω			
VIDSALERT# platform resistors		Rpu1=56Ω, Rpu2=Empty			
Platform resistors tolerances		± 5%			
Route ordering		When routing at minimum spacing route Alert between Data and Clock			



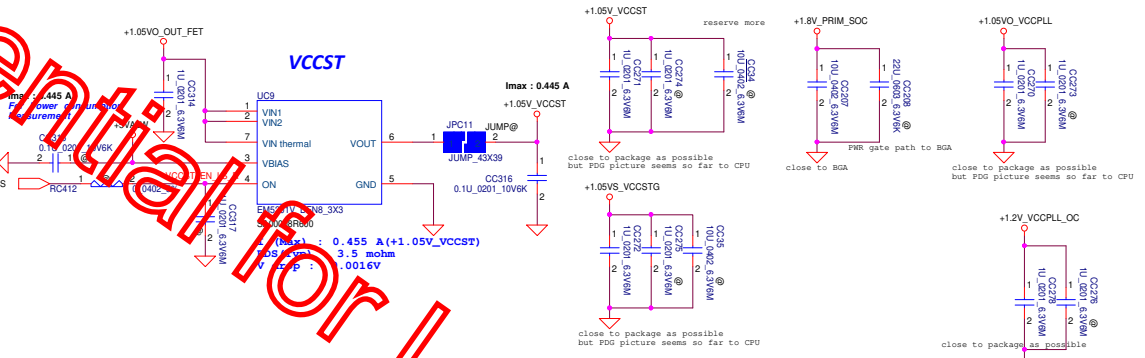
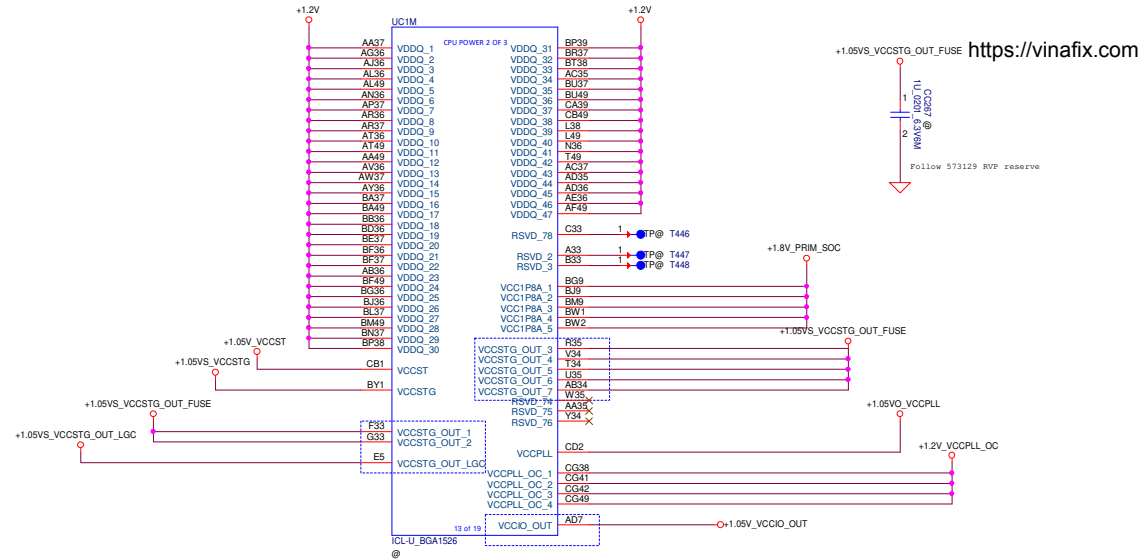
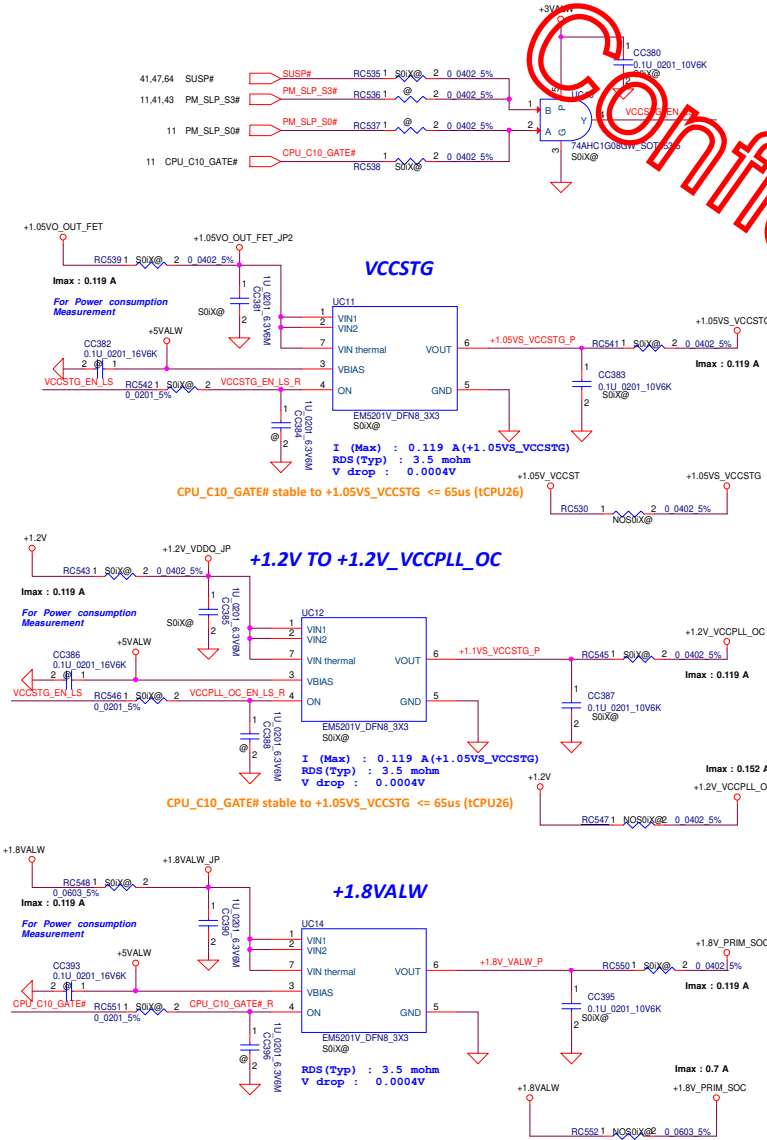
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		LA-LJ551PR02		0.2	
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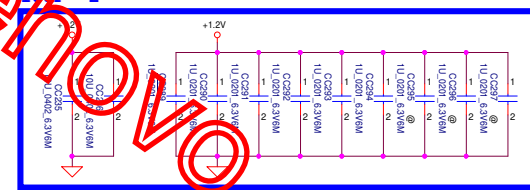
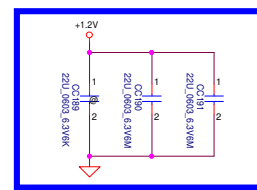
EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 3 (EMI@)
2pF* 3 (EMI@)



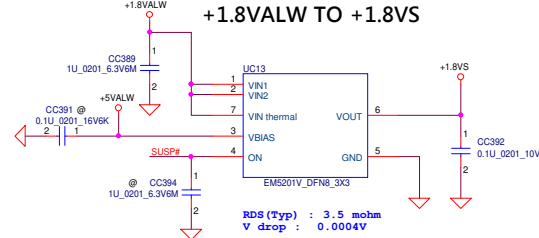
Modern Standby



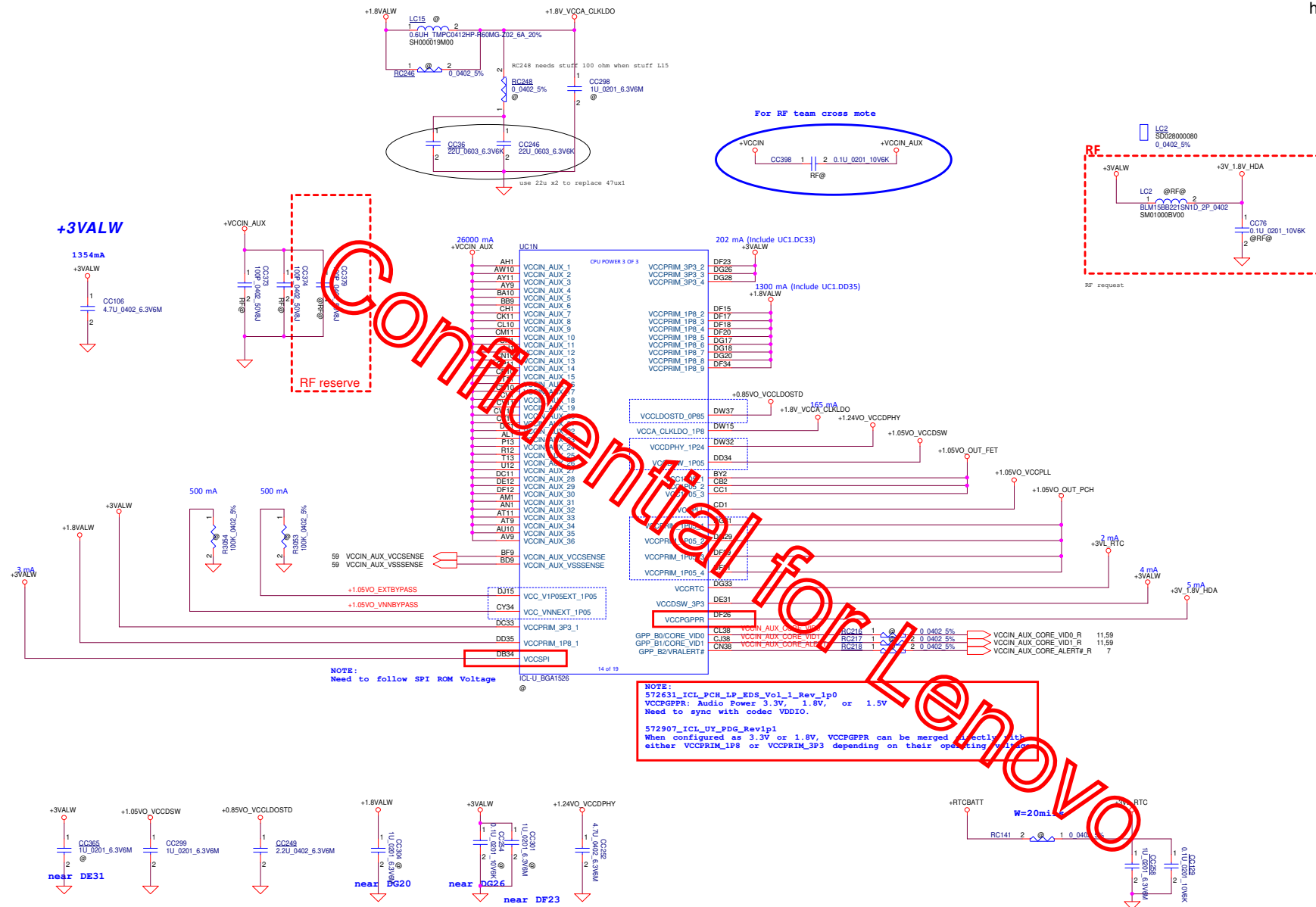
Place on CPU Side
22uF* 2 + 22uF* 1 (Reserved)
Place on opposite of CPU Side
1uF* 6 + 1uF* 3 reserve



+1.8VALW TO +1.8VS



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UC10		
GND 1 OF 3		
A11	VSS_1	VSS_75
A46	VSS_2	VSS_76
BA45	VSS_3	VSS_77
BA47	VSS_4	VSS_78
BB11	VSS_5	VSS_79
BB3	VSS_6	VSS_80
BB7	VSS_7	VSS_81
BC37	VSS_8	VSS_82
BD3	VSS_9	VSS_83
BD38	VSS_10	VSS_84
BD39	VSS_11	VSS_85
BD41	VSS_12	VSS_86
A48	VSS_13	VSS_87
BD42	VSS_14	VSS_88
BD43	VSS_15	VSS_89
BD45	VSS_16	VSS_90
BD49	VSS_17	VSS_91
BD5	VSS_18	VSS_92
BD6	VSS_19	VSS_93
BD7	VSS_20	VSS_94
BE1	VSS_21	VSS_95
BE2	VSS_22	VSS_96
BF3	VSS_23	VSS_97
A49	VSS_24	VSS_98
BF45	VSS_25	VSS_99
BF47	VSS_26	VSS_100
BF7	VSS_27	VSS_101
BG3	VSS_28	VSS_102
BG41	VSS_29	VSS_103
BG7	VSS_30	VSS_104
BH37	VSS_31	VSS_105
BJ1	VSS_32	VSS_106
BJ2	VSS_33	VSS_107
BJ3	VSS_34	VSS_108
AA45	VSS_35	VSS_109
BA41	VSS_36	VSS_110
BA43	VSS_37	VSS_111
BA45	VSS_38	VSS_112
BA49	VSS_39	VSS_113
BJ7	VSS_40	VSS_114
BM11	VSS_41	VSS_115
BM3	VSS_42	VSS_116
BM45	VSS_43	VSS_117
BM47	VSS_44	VSS_118
BM5	VSS_45	VSS_119
AA47	VSS_46	VSS_120
BM6	VSS_47	VSS_121
BM7	VSS_48	VSS_122
BP1	VSS_49	VSS_123
BP2	VSS_50	VSS_124
BP3	VSS_51	VSS_125
BP43	VSS_52	VSS_126
BP7	VSS_53	VSS_127
BR45	VSS_54	VSS_128
BR49	VSS_55	VSS_129
AB11	VSS_56	VSS_130
AB3	VSS_57	VSS_131
AB38	VSS_58	VSS_132
AB39	VSS_59	VSS_133
AB41	VSS_60	VSS_134
A17	VSS_61	VSS_135
AB42	VSS_62	VSS_136
AB43	VSS_63	VSS_137
AB5	VSS_64	VSS_138
AB6	VSS_65	VSS_139
AC45	VSS_66	VSS_140
AC49	VSS_67	VSS_141
AD10	VSS_68	VSS_142
AD11	VSS_69	VSS_143
AD34	VSS_70	VSS_144
AD37	VSS_71	VSS_145
A3	VSS_72	VSS_146
AE6	VSS_73	VSS_147
AF37	VSS_74	VSS_148

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UC1P		
GND 2 OF 3		
BT3	VSS_149	VSS_223
BT39	VSS_150	VSS_224
BT41	VSS_151	VSS_225
BT42	VSS_152	VSS_226
BT43	VSS_153	VSS_227
BT7	VSS_154	VSS_228
BU45	VSS_155	VSS_229
BU47	VSS_156	VSS_230
BV1	VSS_157	VSS_231
BV11	VSS_158	VSS_232
BV2	VSS_159	VSS_233
BV3	VSS_160	VSS_234
BV7	VSS_161	VSS_235
BW3	VSS_162	VSS_236
BW37	VSS_163	VSS_237
BW5	VSS_164	VSS_238
BW6	VSS_165	VSS_239
BW7	VSS_166	VSS_240
BY37	VSS_167	VSS_241
BY45	VSS_168	VSS_242
BY49	VSS_169	VSS_243
C11	VSS_170	VSS_244
C13	VSS_171	VSS_245
C14	VSS_172	VSS_246
C17	VSS_173	VSS_247
C21	VSS_174	VSS_248
C24	VSS_175	VSS_249
C31	VSS_176	VSS_250
C34	VSS_177	VSS_251
C39	VSS_178	VSS_252
C48	VSS_179	VSS_253
C49	VSS_180	VSS_254
C6	VSS_181	VSS_255
CA3	VSS_182	VSS_256
CA37	VSS_183	VSS_257
CA45	VSS_184	VSS_258
CA47	VSS_185	VSS_259
CA49	VSS_186	VSS_260
CB1	VSS_187	VSS_261
CB4	VSS_188	VSS_262
CB7	VSS_189	VSS_263
CC3	VSS_190	VSS_264
CC7	VSS_191	VSS_265
CE37	VSS_192	VSS_266
CE45	VSS_193	VSS_267
CE49	VSS_194	VSS_268
CE9	VSS_195	VSS_269
CG37	VSS_196	VSS_270
CG39	VSS_197	VSS_271
CG43	VSS_198	VSS_272
CG45	VSS_199	VSS_273
CG47	VSS_200	VSS_274
CG9	VSS_201	VSS_275
CH3	VSS_202	VSS_276
CH5	VSS_203	VSS_277
CJ37	VSS_204	VSS_278
CJ42	VSS_205	VSS_279
CJ9	VSS_206	VSS_280
CK45	VSS_207	VSS_281
CK49	VSS_208	VSS_282
OK9	VSS_209	VSS_283
CL37	VSS_210	VSS_284
CL42	VSS_211	VSS_285
CL49	VSS_212	VSS_286
CM45	VSS_213	VSS_287
CM47	VSS_214	VSS_288
CM9	VSS_215	VSS_289
CN3	VSS_216	VSS_290
CN37	VSS_217	VSS_291
CN39	VSS_218	VSS_292
CN5	VSS_219	VSS_293
CP9	VSS_220	VSS_294
CP9	VSS_221	VSS_295
CR32	VSS_222	VSS_296

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UC1Q		
GND 3 OF 3		
DJ33	VSS_297	VSS_362
DJ36	VSS_298	VSS_363
DJ42	VSS_299	VSS_364
DK3	VSS_300	VSS_365
DK4	VSS_301	VSS_366
DK49	VSS_302	VSS_367
DK6	VSS_303	VSS_368
DK8	VSS_304	VSS_369
DL10	VSS_305	VSS_370
DL13	VSS_306	VSS_371
DL44	VSS_307	VSS_372
DL47	VSS_308	VSS_373
DM47	VSS_309	VSS_374
DN15	VSS_310	VSS_375
DN19	VSS_311	VSS_376
DN24	VSS_312	VSS_377
DN31	VSS_313	VSS_378
DN36	VSS_314	VSS_379
DN42	VSS_315	VSS_380
DP45	VSS_316	VSS_381
DR49	VSS_317	VSS_382
DT1	VSS_318	VSS_383
DT10	VSS_319	VSS_384
DT15	VSS_320	VSS_385
DT20	VSS_321	VSS_386
DT27	VSS_322	VSS_387
DT3	VSS_323	VSS_388
DT32	VSS_324	VSS_389
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DT6	VSS_328	VSS_393
DT7	VSS_329	VSS_394
DT8	VSS_330	VSS_395
DU1	VSS_331	VSS_396
DU10	VSS_332	VSS_397
DU15	VSS_333	VSS_398
DU2	VSS_334	VSS_399
DU22	VSS_335	VSS_400
DU32	VSS_336	VSS_401
DU37	VSS_337	VSS_402
DU48	VSS_338	VSS_403
DU49	VSS_339	VSS_404
DU7	VSS_340	VSS_405
DV2	VSS_341	VSS_406
DV44	VSS_342	VSS_407
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DV8	VSS_344	VSS_409
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DW10	VSS_346	VSS_411
DW2	VSS_347	VSS_412
DW20	VSS_348	VSS_413
DW27	VSS_349	VSS_414
DW44	VSS_350	VSS_415
DW46	VSS_351	VSS_416
DW48	VSS_352	VSS_417
DW49	VSS_353	VSS_418
DW7	VSS_354	VSS_419
E11	VSS_355	VSS_420
E34	VSS_356	VSS_421
E37	VSS_357	VSS_422
E38	VSS_358	VSS_423
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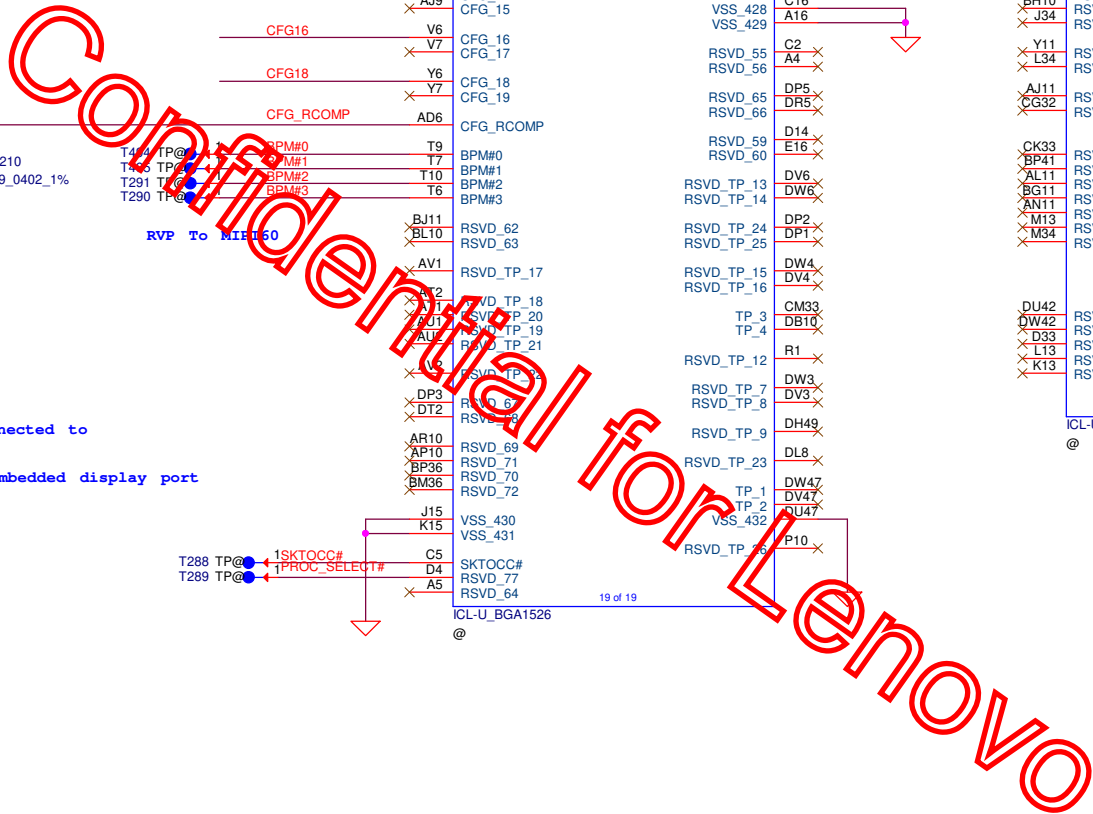
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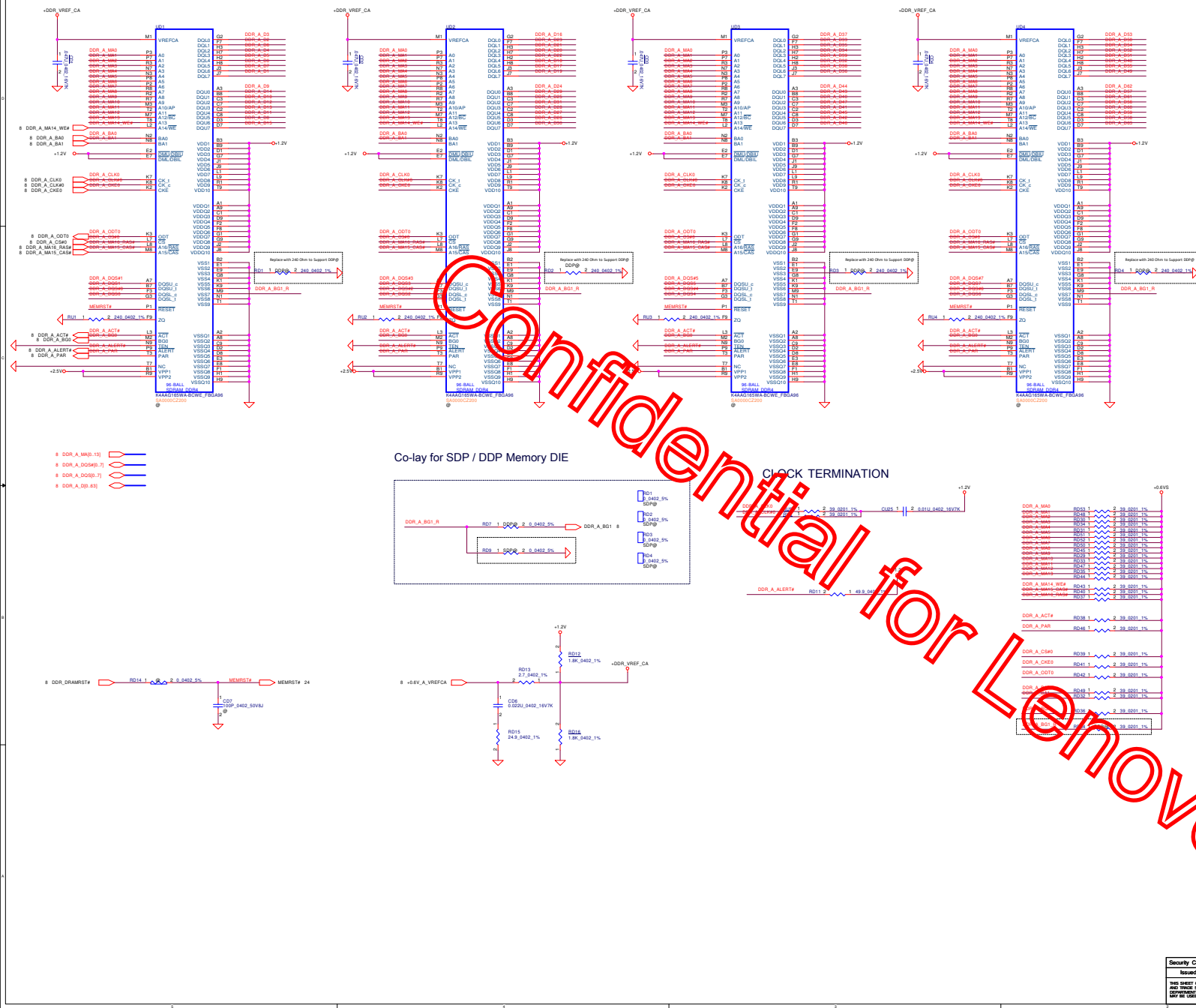
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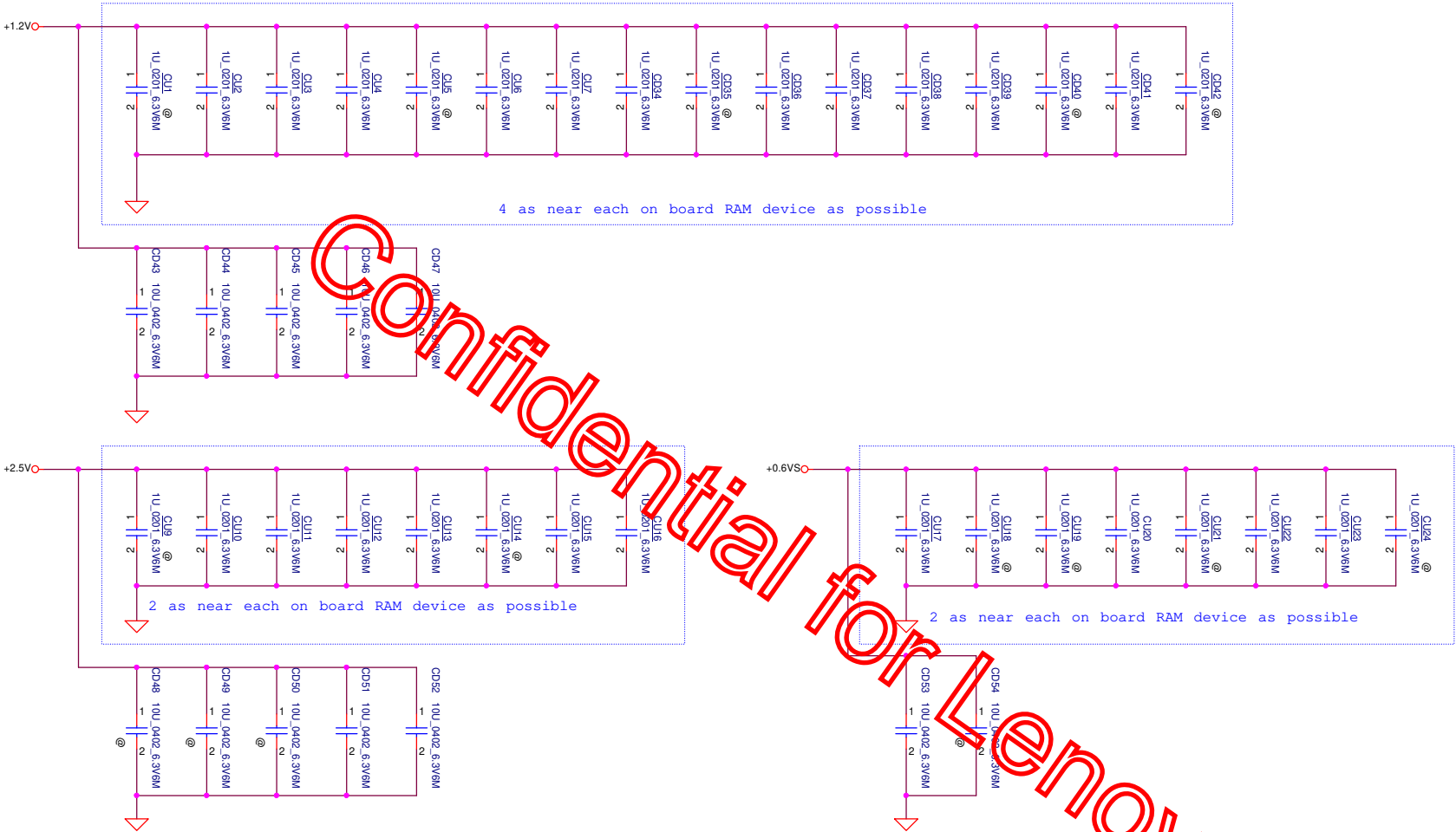
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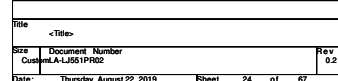
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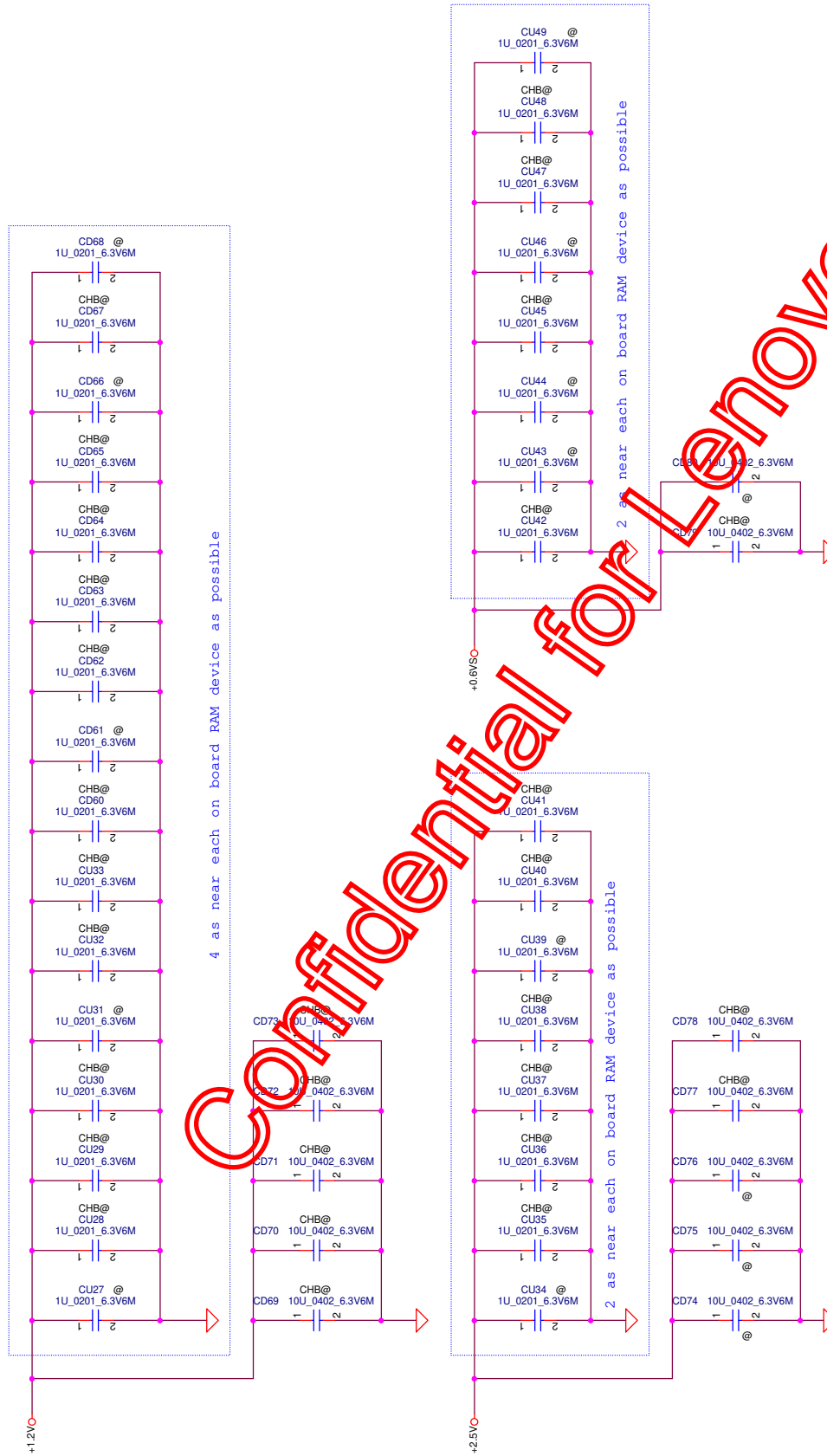


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				Size Document Number	
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<Title>

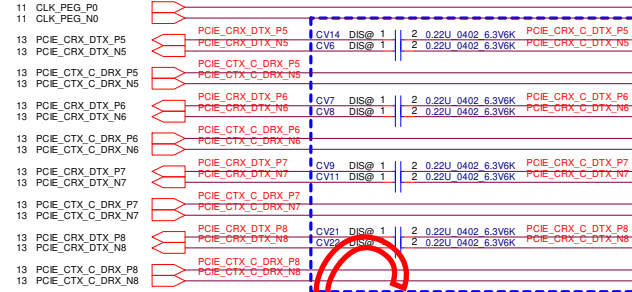
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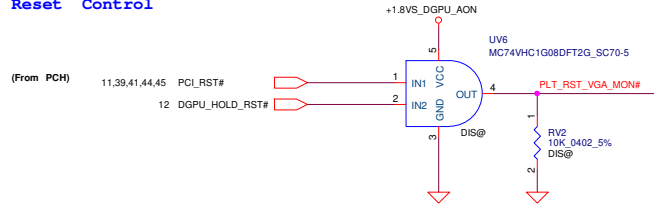
Rev. 0.2

PCIE CLK

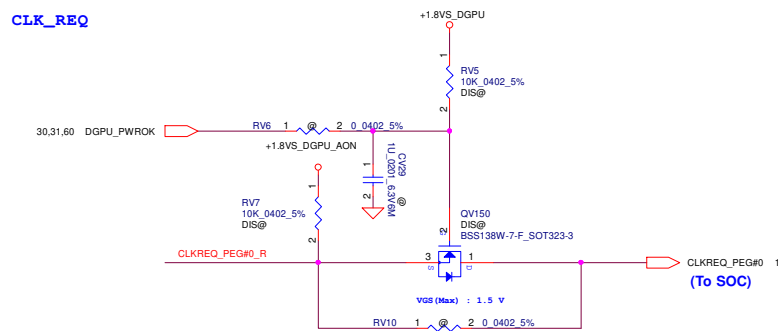


PCIE X4 Bus

Reset Control



CLK_REQ



U1A COMMON

114 PCI_EXPRESS

PEX_WAKE#

PEX_RST#

PEX_CLKREQ#

PEX_REFCLK#

PEX_TX0

PEX_TX0#

PEX_RX0

PEX_RX0#

PEX_TX1

PEX_TX1#

PEX_RX1

PEX_RX1#

PEX_TX2

PEX_TX2#

PEX_RX2

PEX_RX2#

PEX_TX3

PEX_TX3#

PEX_RX3

PEX_RX3#

PEX_TX4

PEX_TX4#

PEX_RX4

PEX_RX4#

PEX_TX5

PEX_TX5#

PEX_RX5

PEX_RX5#

PEX_TX6

PEX_TX6#

PEX_RX6

PEX_RX6#

PEX_TX7

PEX_TX7#

PEX_RX7

PEX_RX7#

PEX_TX8

PEX_TX8#

PEX_RX8

PEX_RX8#

PEX_TX9

PEX_TX9#

PEX_RX9

PEX_RX9#

PEX_TX10

PEX_TX10#

PEX_RX10

PEX_RX10#

PEX_TX11

PEX_TX11#

PEX_RX11

PEX_RX11#

PEX_TX12

PEX_TX12#

PEX_RX12

PEX_RX12#

PEX_TX13

PEX_TX13#

PEX_RX13

PEX_RX13#

PEX_TX14

PEX_TX14#

PEX_RX14

PEX_RX14#

PEX_TX15

PEX_TX15#

PEX_RX15

PEX_RX15#

PEX_TX16

PEX_TX16#

PEX_RX16

PEX_RX16#

PEX_TX17

PEX_TX17#

PEX_RX17

PEX_RX17#

PEX_TX18

PEX_TX18#

PEX_RX18

PEX_RX18#

PEX_TX19

PEX_TX19#

PEX_RX19

PEX_RX19#

PEX_TX20

PEX_TX20#

PEX_RX20

PEX_RX20#

PEX_TX21

PEX_TX21#

PEX_RX21

PEX_RX21#

PEX_TX22

PEX_TX22#

PEX_RX22

PEX_RX22#

PEX_TX23

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PEX_RX23

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PEX_TX24

PEX_TX24#

PEX_RX24

PEX_RX24#

PEX_TX25

PEX_TX25#

PEX_RX25

PEX_RX25#

PEX_TX26

PEX_TX26#

PEX_RX26

PEX_RX26#

PEX_TX27

PEX_TX27#

PEX_RX27

PEX_RX27#

PEX_TX28

PEX_TX28#

PEX_RX28

PEX_RX28#

PEX_TX29

PEX_TX29#

PEX_RX29

PEX_RX29#

PEX_TX30

PEX_TX30#

PEX_RX30

PEX_RX30#

PEX_TX31

PEX_TX31#

PEX_RX31

PEX_RX31#

PEX_TX32

PEX_TX32#

PEX_RX32

PEX_RX32#

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PEX_RX33

PEX_RX33#

PEX_TX34

PEX_TX34#

PEX_RX34

PEX_RX34#

PEX_TX35

PEX_TX35#

PEX_RX35

PEX_RX35#

PEX_TX36

PEX_TX36#

PEX_RX36

PEX_RX36#

PEX_TX37

PEX_TX37#

PEX_RX37

PEX_RX37#

PEX_TX38

PEX_TX38#

PEX_RX38

PEX_RX38#

PEX_TX39

PEX_TX39#

PEX_RX39

PEX_RX39#

PEX_TX40

PEX_TX40#

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PEX_TX74

GPU_Decoupling CAPs @ Power Page

Table 4. Frame Buffer Core and IO Decoupling and Filtering

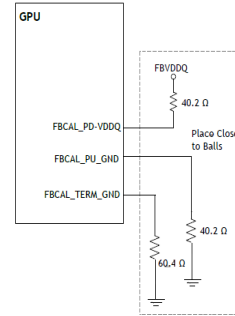
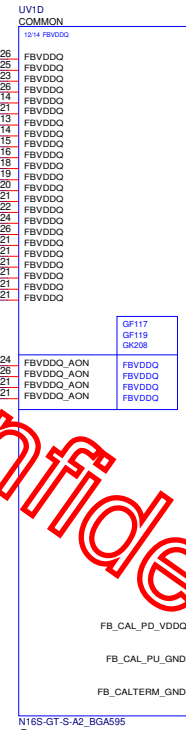
GPU	Capacitor Type	Footprint	N16	N17	Location
FBVDD/Q Supply Rail for GDDR5					
GB2B-64, GB2C-64	0.1 μ F	X7R 0402	2	0	Under GPU
	1 μ F	X7R 0603	2	8	Under GPU
	4.7 μ F	X6S 0603	2	0	Under GPU
	10 μ F	X6S 0603	0	2	Under GPU
	10 μ F	X6S 0603	1	1	Near GPU
	22 μ F	X6S 0603W	1	3	Near GPU

GPU Package Type	Capacitor Type	Footprint	Population	Location	
GB2B-64/GB2-64 GDDR5	0.1 μ F	X7R 0402	2	2	Under GPU
	1 μ F	X7R 0603	2	2	Under GPU
	4.7 μ F	X6S 0603	2	2	Under GPU
	10 μ F	X5R 0805	1	1	Near GPU
	22 μ F	X5R 0805	1	1	Near GPU

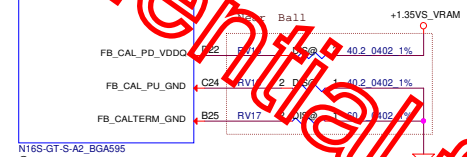
NC (N17: GPCPLL_AVDD) Supply Rail					
GB2C-64	0.1 μ F	X7R 0402	N/A	1	Under GPU
	4.7 μ F	X6S 0603	N/A	1	Near GPU
	22 μ F	X6S 0805	N/A	1	Near GPU
Bead Type					
L=30 Ω (ESR=0.010 Ω)	0603	N/A	1	Near GPU	

Place near GPU

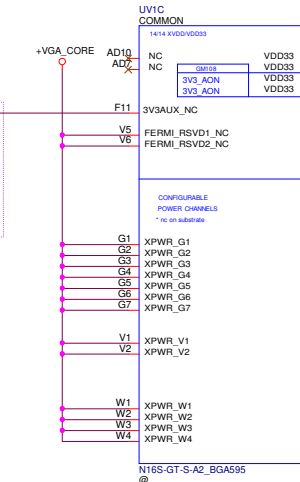
Place under GPU



Note: Use only 1% resistors for driver calibration



N16S-GT-S-A2_BGA595



N16S-GT-S-A2_BGA595

** XPWR pins are configurable.

These pins are not connected on the substrate.
Therefore, XPWR pins can be assigned as needed,
to improve Top layer routing, power delivery.

+VGA CORE

Voltage by GPU SKU

UVIE COMMON

10/14 NVDDQ

K10

VDD

K12

VDD

K14

VDD

K16

VDD

K18

VDD

K20

VDD

K22

VDD

K24

VDD

K26

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K28

VDD

K30

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K54

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K56

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K58

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K60

VDD

K62

VDD

K64

VDD

K66

VDD

UVIF COMMON

10/14 GND

A2

GND

A2

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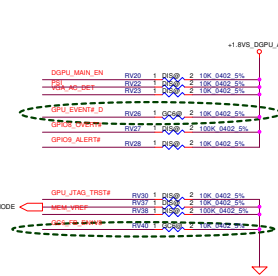
M79

GND

GPU Package	Rail	Capacitor Type	Footprint	Population	Location
GB2B-64	3V3_MAIN	0.1 μ F X6S	0402 2	2	Under GPU
GB2B-64	3V3_MAIN	1 μ F X5R	0603 1	1	Near GPU
GB4B-128		4.7 μ F X5R	0603 1	1	Near GPU
GB3B-256					
GB2B-64	3V3_MAIN	0.1 μ F X6S	0402 1	1	Under GPU
GB2B-64	3V3_MAIN	1 μ F X5R	0603 1	1	Near GPU
GB4B-128		4.7 μ F X5R	0603 1	1	Near GPU
GB3B-256					

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

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Size	Document Number	Rev	0.2
Date:	Thursday, August 22, 2019	Sheet	28 of 67

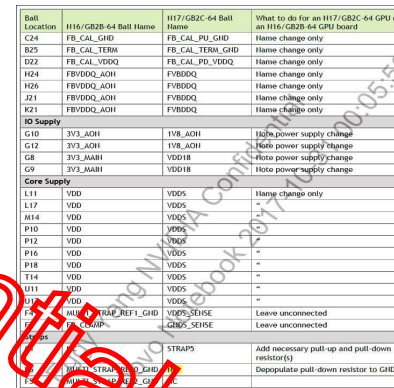


<https://vinafix.com>

10.2.2 I²C Slave Address

16.3.3 Internal Thermal Sensor Interface

The internal thermal sensor can be accessed through the PCS interface as described in the FC chapter. This interface is compliant with the System Management Bus (SMBus) Specification (Version 2.0). The interface supports PEC and SMBus Timeout as well as Read Byte and Read Byte with PEC. Writes to the internal thermal sensor registers through the FC interface by the system is not supported. The default port address to access the internal thermal sensor over the FC is 0x9E. Table 16-1 describes the byte-wise register accessible through the FC interface.



GPIO Name	GPIO Name	Functional Description	Not Terminated
GP00	GPIO_PU_0	FX Extnar for GCA-2.0, Open Source	No pull-up/pull-down
GP01	MEX_VDD_CTL_0	Memory voltage control	Pull-up/pull-down to 3V3, 10k pull-down
GP02	LOC_PW_BW	Panel Backlight PWM Brightness Control	No pull-up/pull-down
GP03	LOC_VCC	Panel Power Enable	No pull-up/pull-down
GP04	LOC_PDA	Panel Power Disable	10k pull-down
GP05	GPIO_3V3_A0H_0	3V3 A0H pin connecting to GCA-2.0, Open Source	No pull-up/pull-down to 3V3, 10k pull-down
GP06	GPIO_VID_0	Open Drain	No pull-up/pull-down to 3V3, 10k pull-down
GP07	SPD_VID0	3V3 Vision LED Input	No pull-up/pull-down to 3V3, 10k pull-down
GP08	SIX_RX_RXD_H0H_1	System side Thermal monitor	No pull-up/pull-down to 3V3, 10k pull-down
GP09	THRM_ALERT_0	Active Low Thermal Alert, Open Drain	No pull-up/pull-down to 3V3, 10k pull-down
GP10	MEX_VREF_CTL_0	Memory Voltage Reference Control	No pull-up/pull-down to 3V3, 10k pull-down
GP11	GPIO_3V3_A0H_1	3V3 A0H pin connecting to GCA-2.0, Open Source	No pull-up/pull-down to 3V3, 10k pull-down
GP12	PWR_LED_1	MCU-Driven LED power supply hardware input	No pull-up/pull-down to 3V3, 10k pull-down
GP13	PWA_0	Power Sense Detector	10k pull-up to 3V3, 10k pull-down
GP014	HPO_A	Hot Plug Detect for HPA used as DisplayPort, HPA used as DisplayPort	See Figure 12-1
GP015	HPO_C	Hot Plug Detect for HPC	See Figure 12-1
GP016	FRAME_LOCK_1	Hot Plug Low Frame, Open Drain	10 kΩ pull-up to 3V3, 10k pull-down for GDS-0
GP017	HPO_D	Hot Plug Detect for HPD	See Figure 12-1
GP018	HPO_E	Hot Plug Detect for HPE	See Figure 12-1
GP019	HPO_F/HPO_B	Hot Plug Detect for HFF or for HFB when used as DisplayPort	See Figure 12-1
GP020	Reserved		
GP021	GPIO_3V3_A0H_VDD0H	GPIO PWR reset control, Open Drain	No pull-up/pull-down to 3V3, 10k pull-down
OVERT	OVERT	Cathodisc Over Temperature	No pull-up/pull-down to 3V3, 10k pull-down



Notes:

1. For N175-G0/G2/G3/G4, the maximum allowable memory case temperature is 83 °C.
2. N175-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N175-G1.

Table 5.3 RAMCFG

Strap Plus see Note			RAMC (see Note) Number
STRAP2	STRAP1	STRAP0	(see Memory XVI) (see memory code corresponding to the memory number)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)

Row Index	Setup Pins			Resulting SDR ₁ EXPOSED Enablements			
	ROM_S0	ROM_S1	ROM_SCL	SDR ₁ EXPOSED	SDR ₂ EXPOSED	SDR ₁ EXPOSED	SDR ₂ EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	ENABLED
13	L	H	L	ENABLED	ENABLED	disabled	disabled
12	L	H	H	ENABLED	ENABLED	disabled	disabled
11	H	L	L	ENABLED	ENABLED	disabled	disabled
10	H	L	H	ENABLED	ENABLED	disabled	disabled
9	H	H	L	ENABLED	disabled	disabled	disabled
8	H	H	H	disabled	disabled	disabled	disabled

(L) other Strata Configurations (H) other Strata Configurations

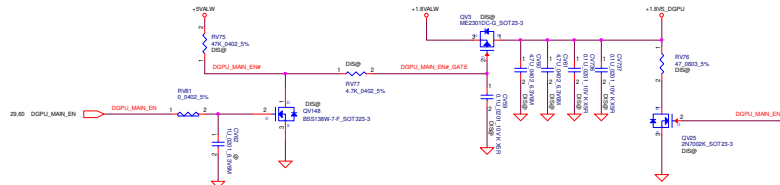
(disabled) do not configure (disabled) do not configure

Strap Pins			Functions Selected by This Strapping			
STRAPS	STRAP4	STRAP3	SMR_ALT_ADDR	DEV0_SEL	PCIE_CFG	VGA_DEVIC
L	L	L	0	0	0	0
L	L	H	0	0	0	0
L	H	H	0	0	1	0
L	H	L	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1

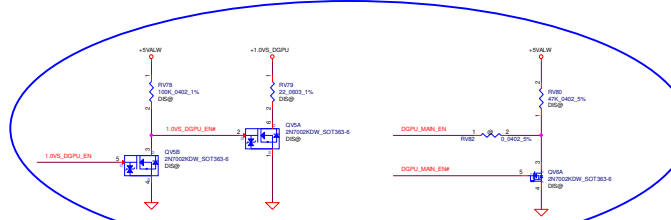
ROM_SO	ROM_SI	ROM_SCLK	STRAP5	STRAP4	STRAP3
 RV2468 DISQ 100K_0402_5%	 RV2469 DISQ 100K_0402_5%	 RV2471 DISQ 100K_0402_5%	 RV443 DISQ 100K_0402_5%	 RV385 DISQ 100K_0402_5%	 RV387 DISQ 100K_0402_5%

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			Date: Thursday, April 15, 2021 23:01:01	

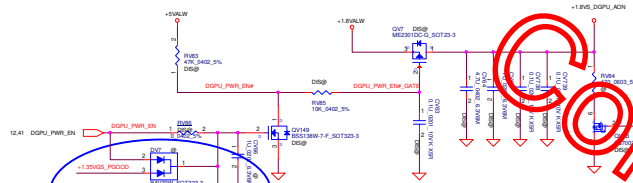
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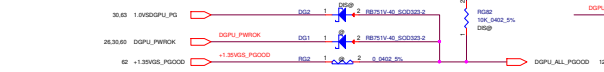
Discharger



+1.8VALW to +1.8VS_DGPU_AON



Reserve for GPU sequence tuning



Reserve for GPU sequence tuning

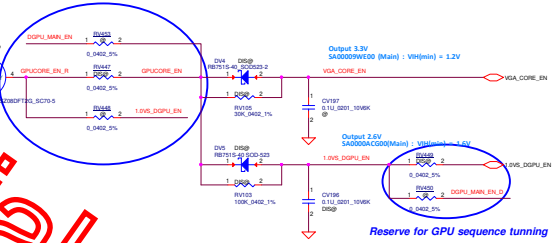


Table 5. EDP-Continuous³

Products	VRAM Type	GPU Core	GPU FBIO		FB Total ^{1,5}		1.05V Total ⁴	3.3V Total
		—	1.5V ⁴	1.35V ⁴	1.5V ⁴	1.35V ⁴	1.05V ⁴	3.3V ⁴
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N165-GTR	GDDR5	26.5	—	2.0	—	4.2	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

GPU	Capacitor Type	Footprint	Population	N16	N17	Location
N16 3V3_MAIN (N17 VDD18) Supply Rail						
GB2B-64	0.1 µF X7R	0402	2	2	2	Under GPU
GB2C-64	1.0 µF X6S	0603	1	1	1	Under GPU
	4.7 µF X6S	0603	1	1	1	Near GPU
N16 3V3_AON (N17 VBS_AON) Supply Rail						
GB2B-64	0.1 µF X7R	0402	1	1	1	Under GPU
GB2C-64	1.0 µF X6S	0603	1	1	1	Near GPU
	4.7 µF X6S	0603	1	1	1	Near GPU

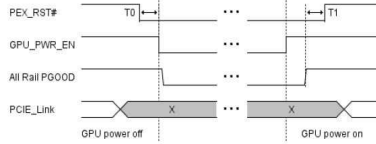
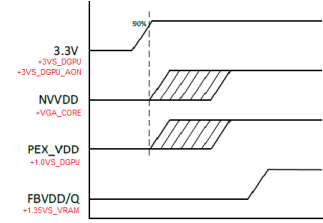


Figure 18-7. Optimus Entry/Exit Timing Diagram

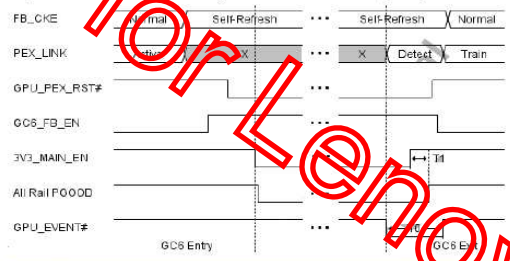
Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# deassertion	0.1	5	ms



Note:
 • 3.3V includes all rails powered at 3.3V. PEVD includes all rails that are shared on 1.05V/1.0V.
 • The ramp time for any rail must be more than 40 µs and is recommended to be less than 2 ms.

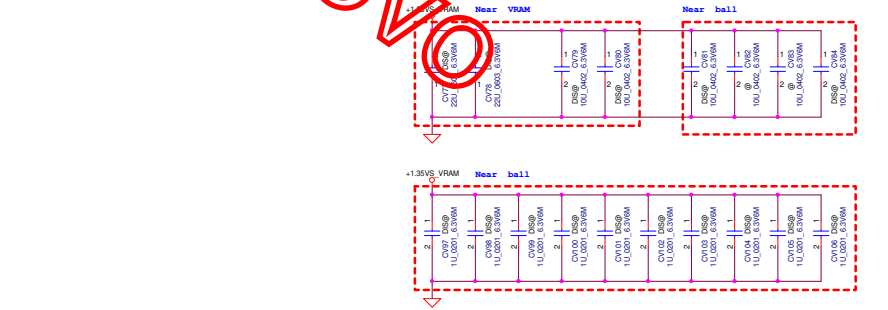
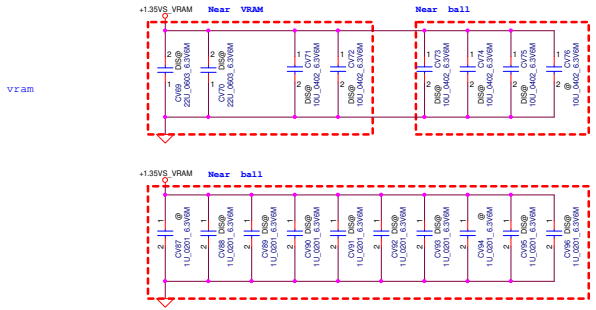
Figure 18-12. OptiV 2.0 Entry/Exit Sequence Timing Diagram



Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	µs
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

Note:
 • ALL Rail PGOOD=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
 • During GC6 exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
 • All delays should be minimized to increase time spent in GC6 for maximum power saving.
 • The entire entry/exit sequence must complete within 200 ms.

Table 7-4. GDDR5 Mode H Mapping

[illegible]

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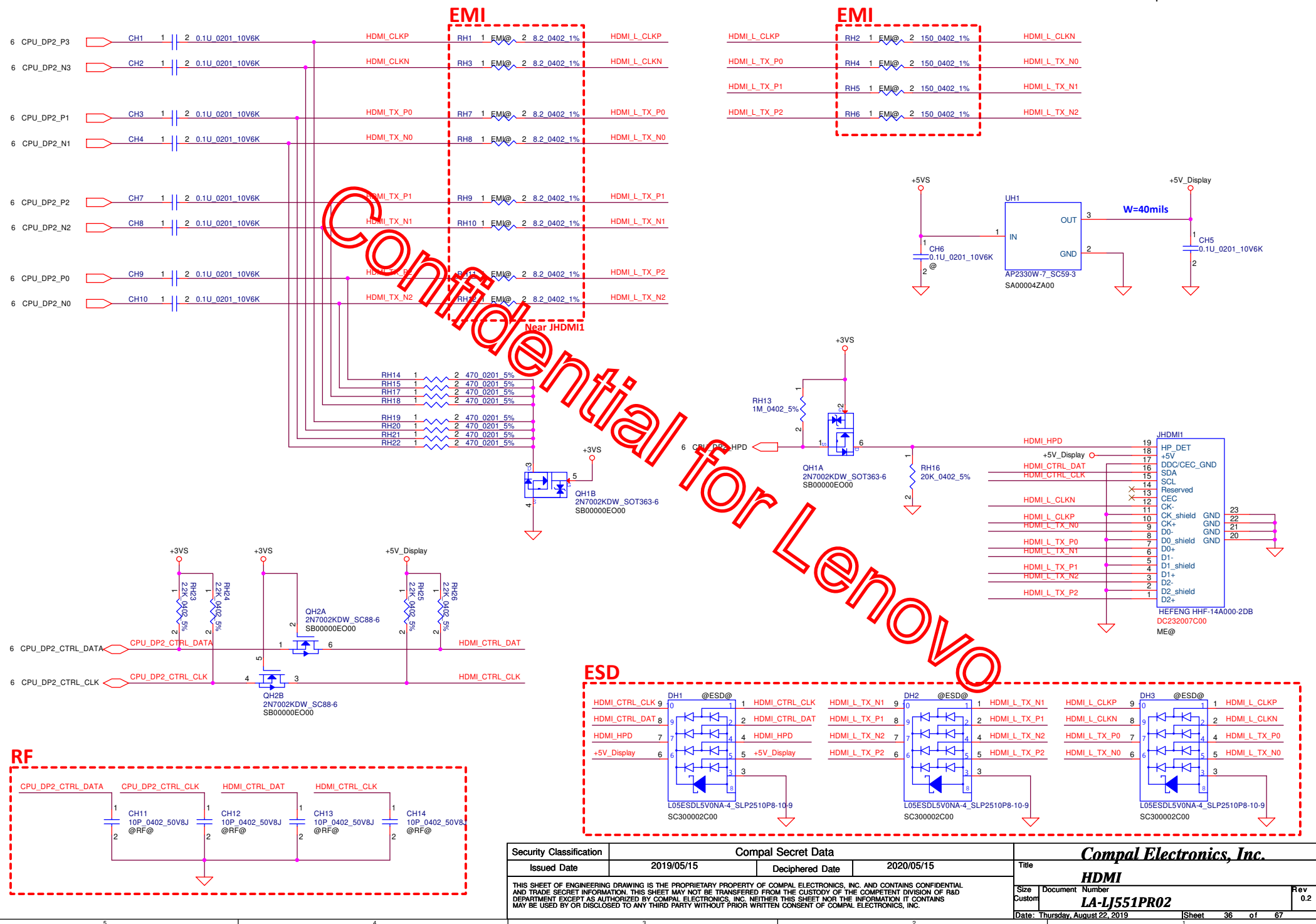
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HDMI

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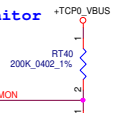


Slave Address setting

Slave Addr	Na	Nb	Nc	Nd	Ne
addr0:0x0C	NC	10K			<0.2V
addr1:0x0E	75K	10K			>=0.2V&<0.6V
addr2:0x00	33K	10K			>=0.6V&<1.0V
addr3:0x02	10K	10K			>=1.0V

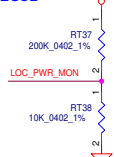
It's used for SMBUS slave addr0/1/2/3 setting during power on initialization.

VBUS Voltage/current Monitor

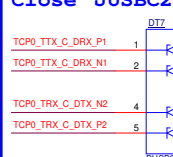


Local PWR Voltage Monitor

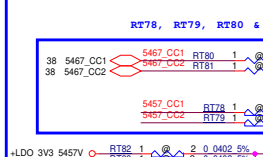
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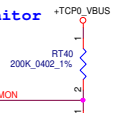
Close JUSBC2



USB TYPE-C ESD Protection



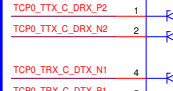
VBUS Discharge



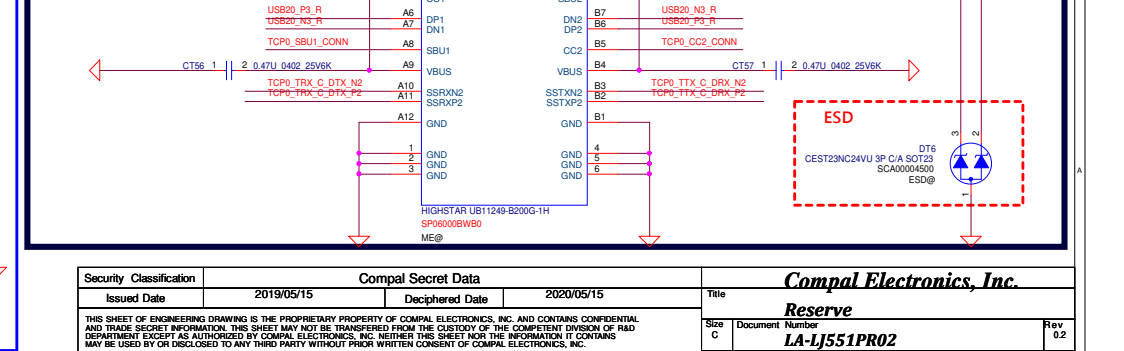
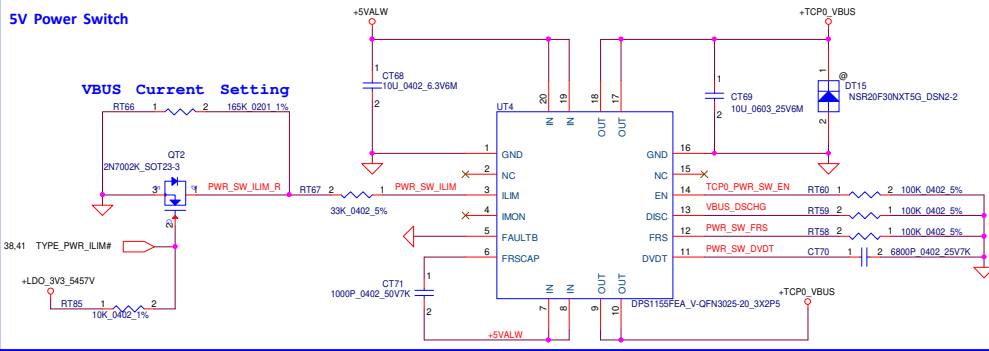
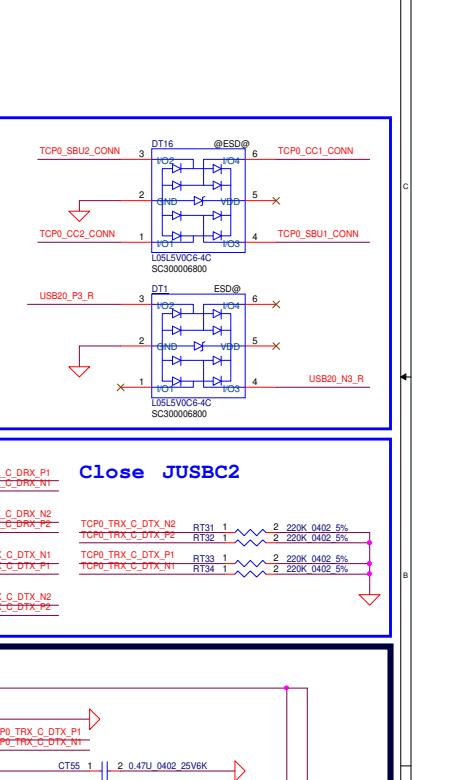
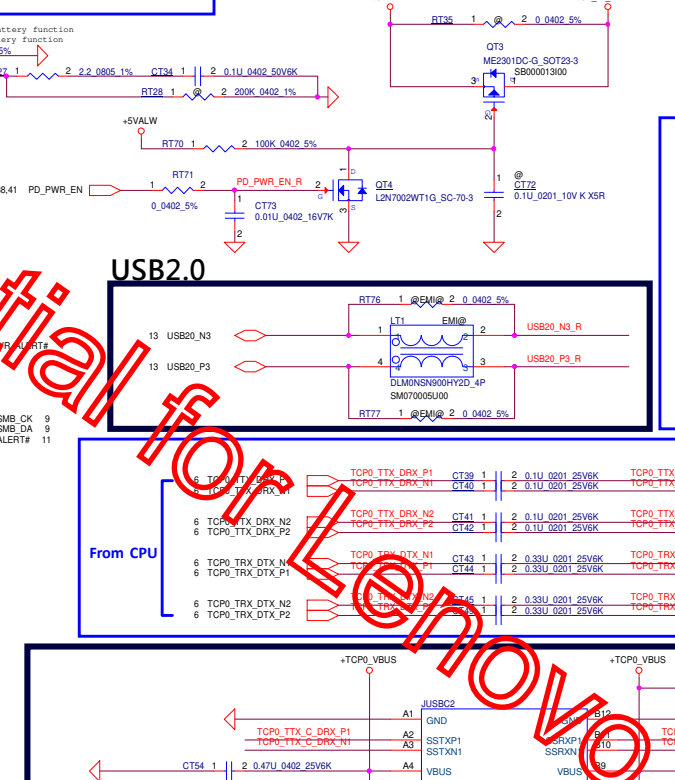
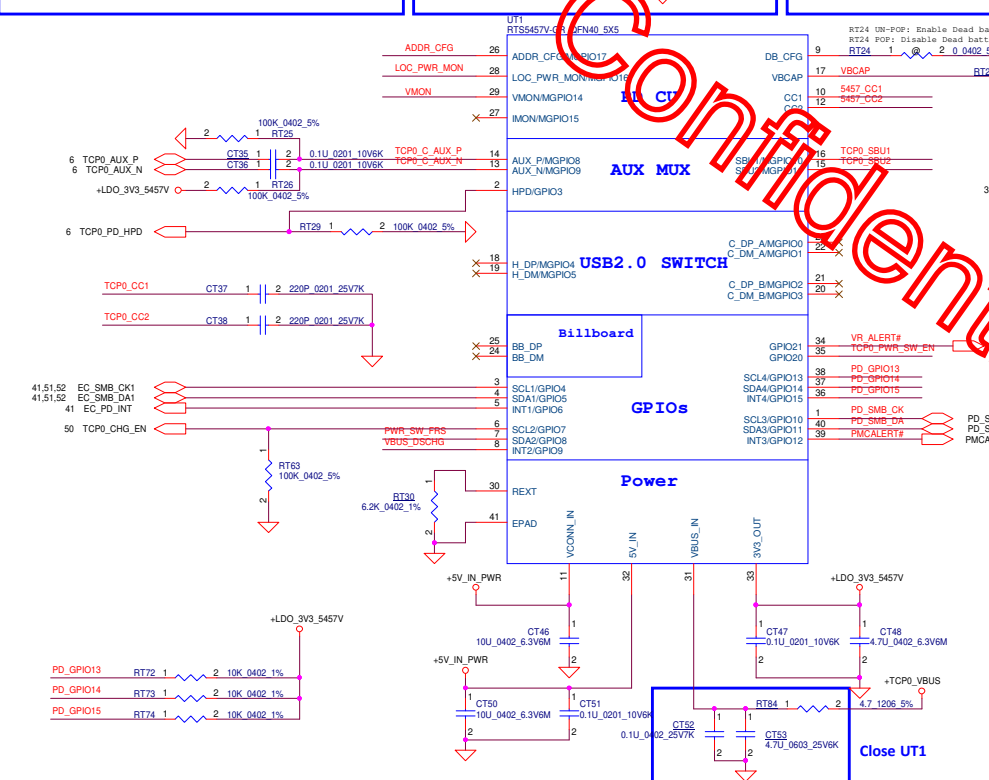
VBUS Discharge



Close JUSBC2



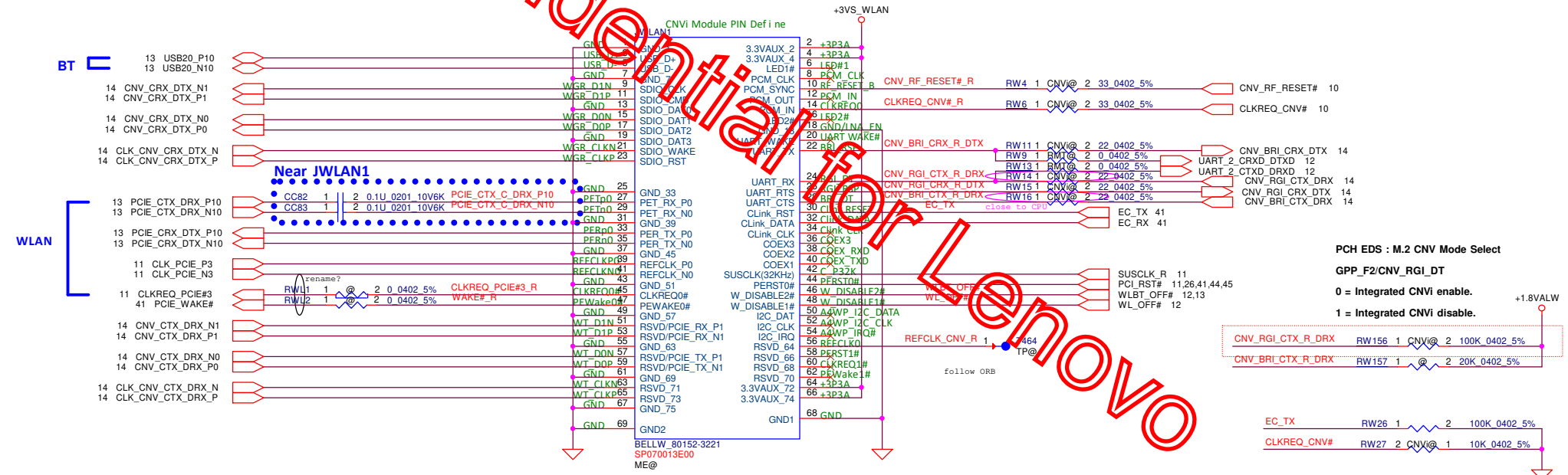
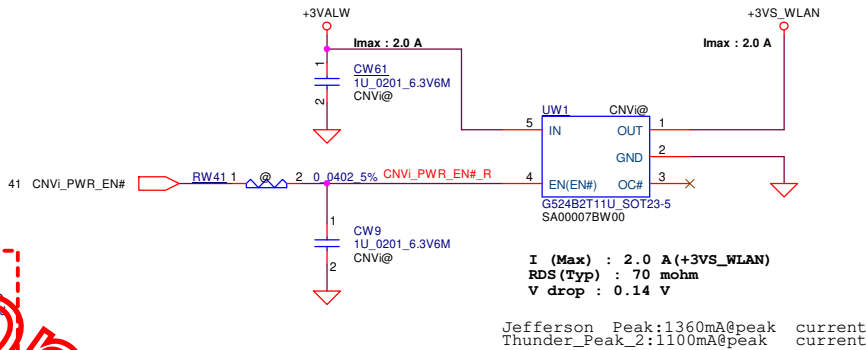
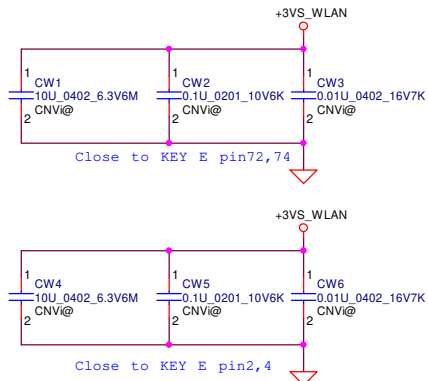
USB TYPE-C ESD Protection



NGFF WLAN / BT (Key E)

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]

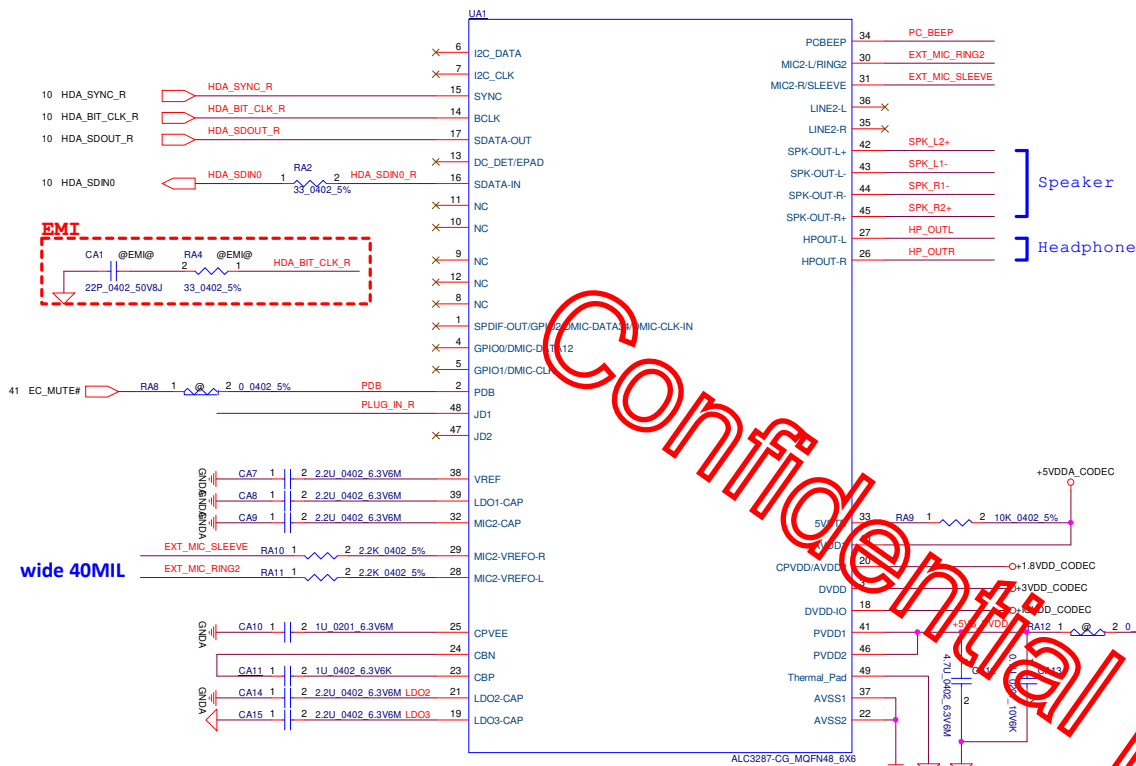
https://vinafix.com



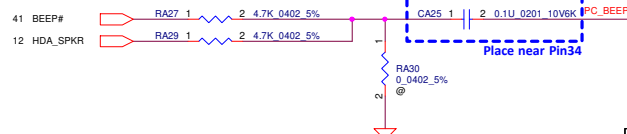
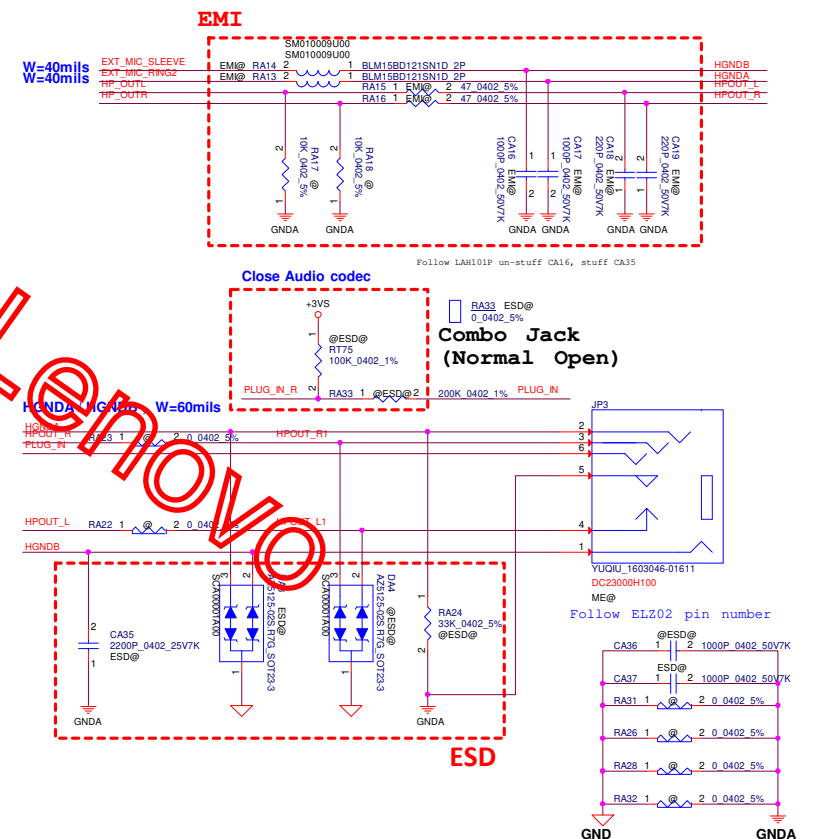
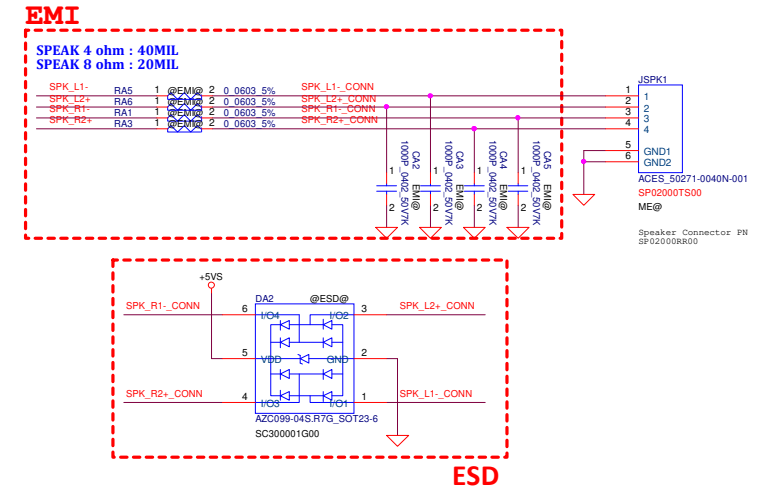
Note: The real behavior of BT_DISABLE are BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON

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Size	Document	Number	Rev	LA-LJ551PR02	
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ALC3287



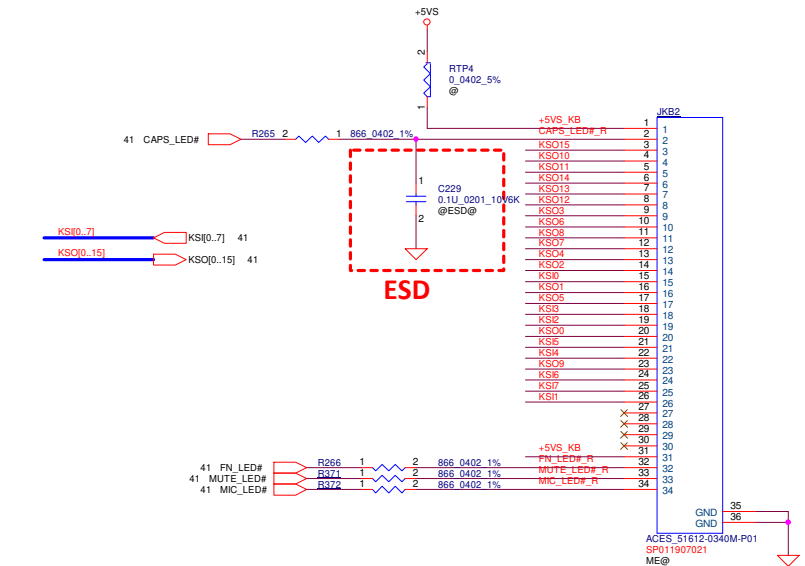
<https://vinafix.com>



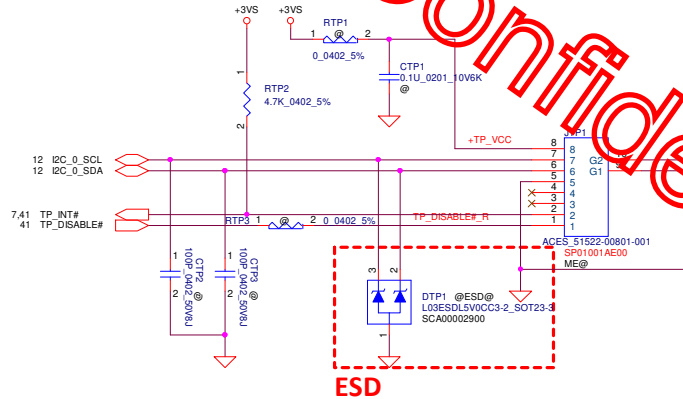
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Issued Date	2019/05/15	Deciphered Date	2020/05/15	Title	
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Keyboard

https://vinafix.com



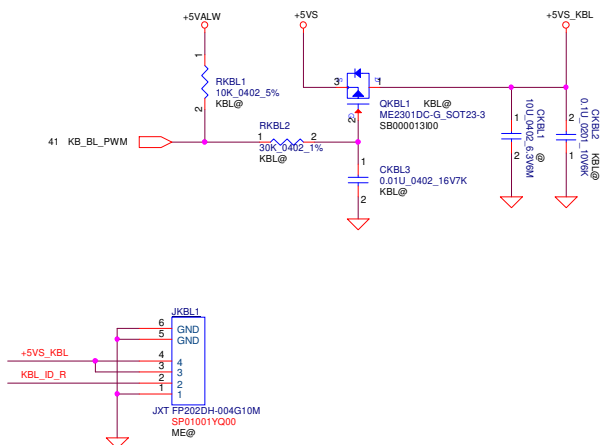
Touch Pad



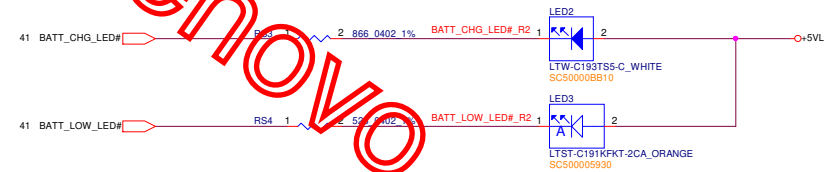
Keyboard Backlight

Keyboard BackLight_SELECT

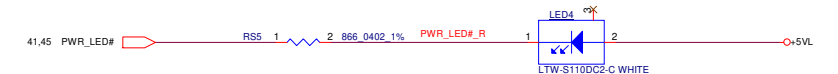
Function	KBL_ID
KBL	0
NO KBL	1



BATT LED

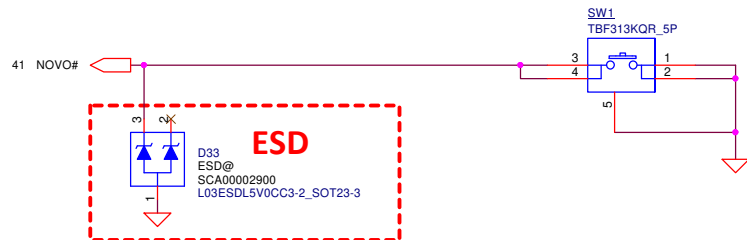


Status LED

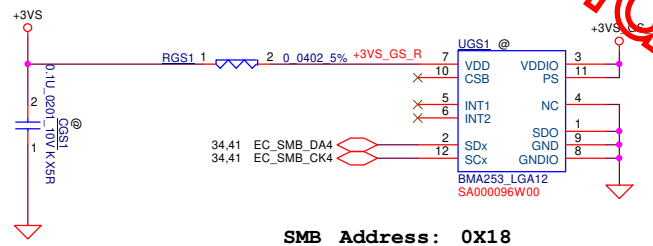


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Deciphered Date				2020/05/15				KB / LED / TP / LID			
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Size				Document Number				Rev			
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67											

NOVO Button

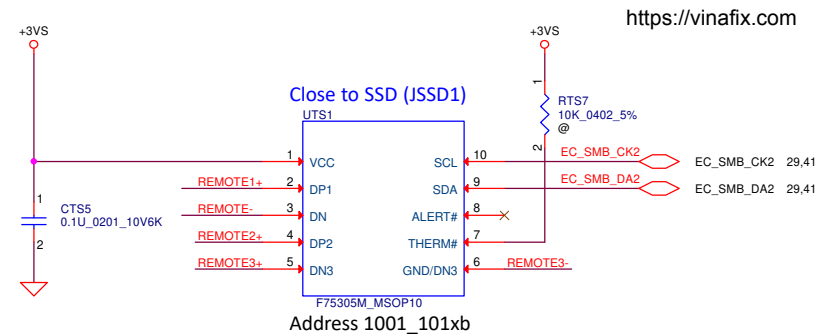


G-Sensor

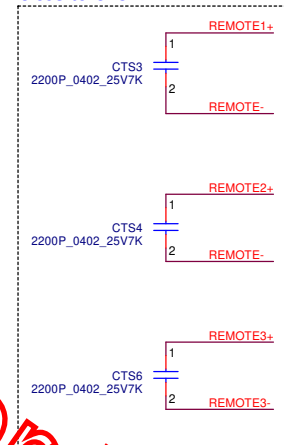


SMB Address: 0X18

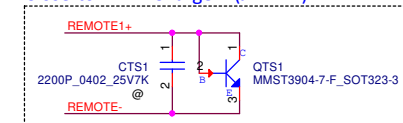
Thermal Sensor



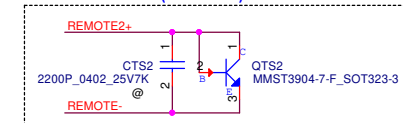
Close to UTS1



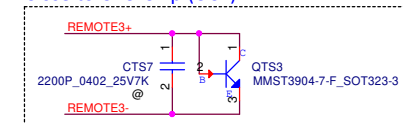
Close to BATT Charger (JBATT1)



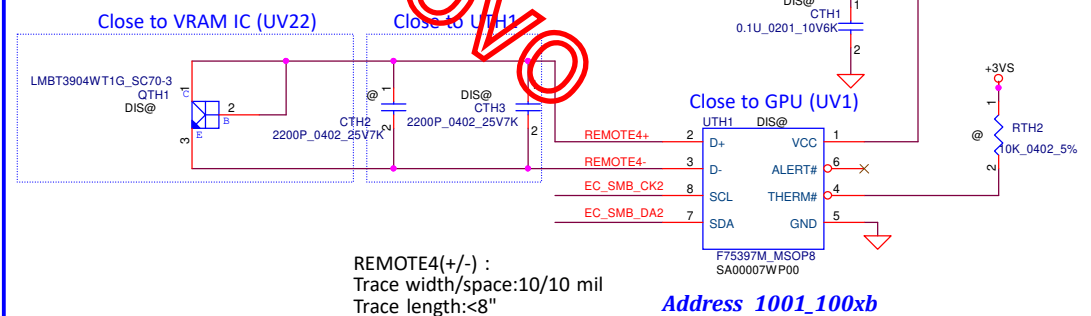
Close to WLAN (JWLAN1)



Close to CPU Chip (UC1)



REMOTE1,2,3 (+/-) :
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Trace length:<8"

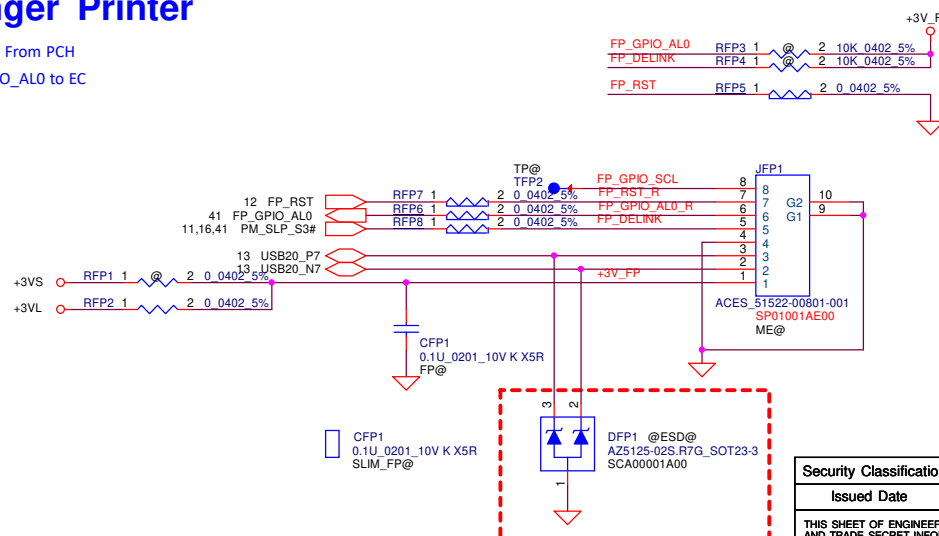


REMOTE4(+/-) :
Trace width/space:10/10 mil
Trace length:<8"

Address 1001_100xb

Finger Printer

FP_RST From PCH
FP_GPIO_AL0 to EC



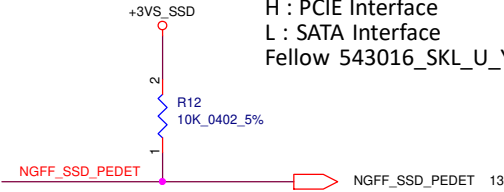
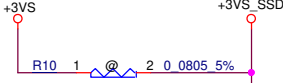
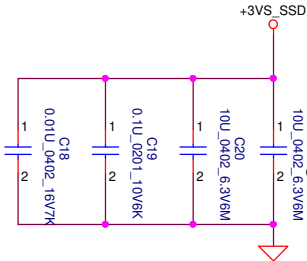
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Size	Document Number	Rev		Date: Thursday, August 22, 2019	
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SSD (TYPE M)

SSD PCIE

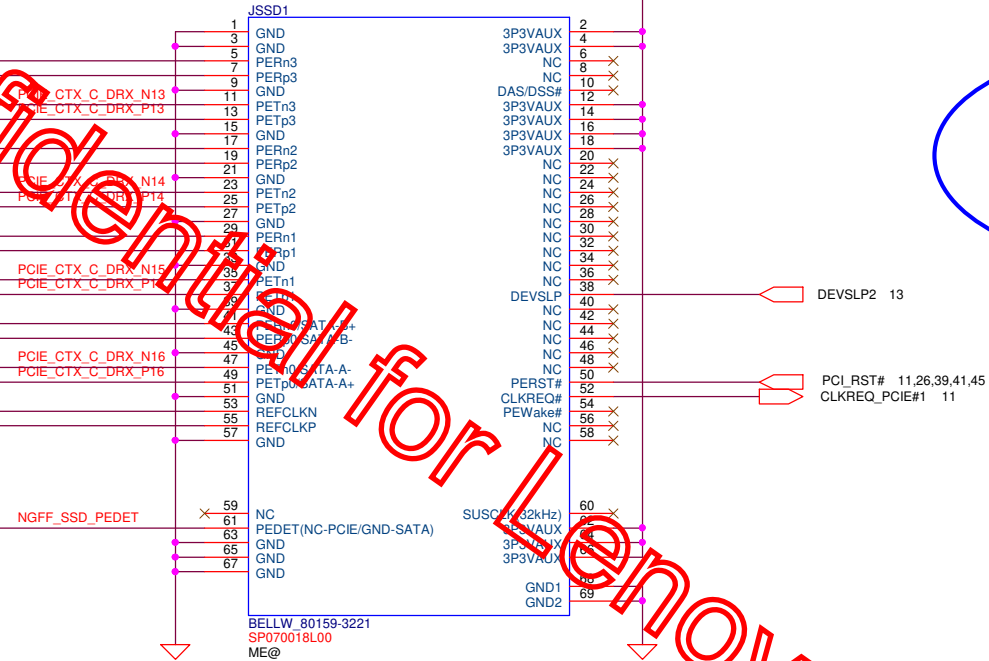
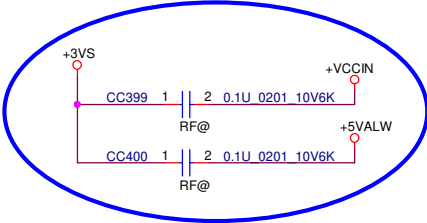
SSD SATA

- 13 PCIE_CRX_DTX_N13
- 13 PCIE_CRX_DTX_P13
- 13 PCIE_CTX_DRX_N13
- 13 PCIE_CTX_DRX_P13
- 13 PCIE_CRX_DTX_N14
- 13 PCIE_CRX_DTX_P14
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- 13 PCIE_CTX_DRX_P15
- 13 PCIE_CRX_DTX_N16
- 13 PCIE_CRX_DTX_P16
- 13 PCIE_CTX_DRX_N16
- 13 PCIE_CTX_DRX_P16
- 11 CLK_PCIE_N1
- 11 CLK_PCIE_P1



NGFF_SSD_PEDET#
H : PCIe Interface
L : SATA Interface
Fellow 543016_SKL_U_Y_PDG_0_9

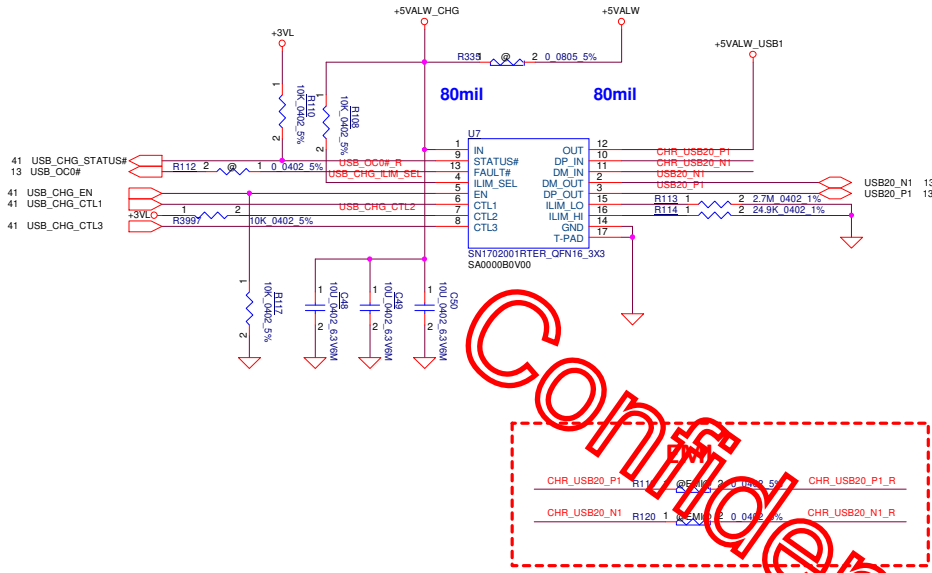
For RF team cross mote



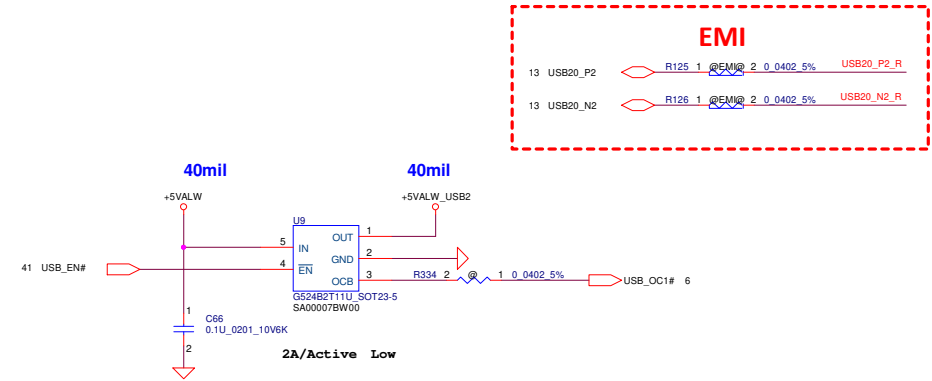
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				Size	Document Number
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USB3.0_Port (AOU_Port)

https://vinafix.com

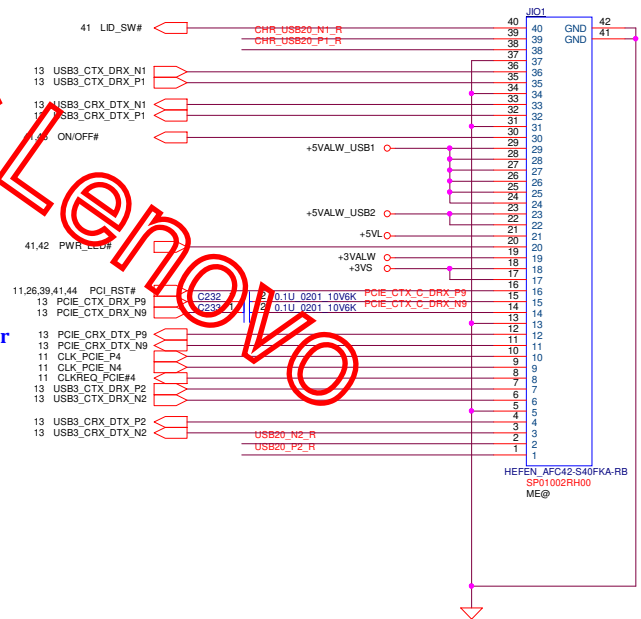


USB3.0_Port (Non-AOU_Port)



10 CONN

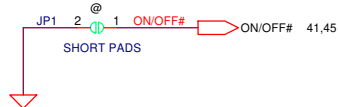
Card Reader



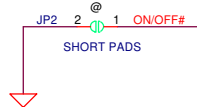
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Size	Document	Number	Rev	Date: Thursday, August 22, 2019	
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ON/OFF# SHORT PAD

TOP side

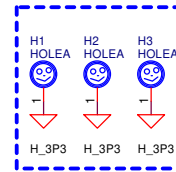


BOTT side

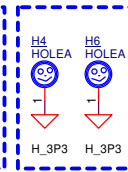


SCREW

CPU



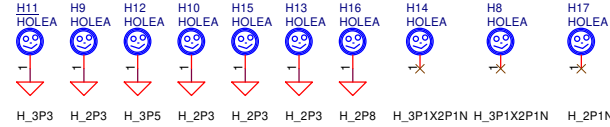
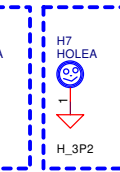
GPU



WLAN

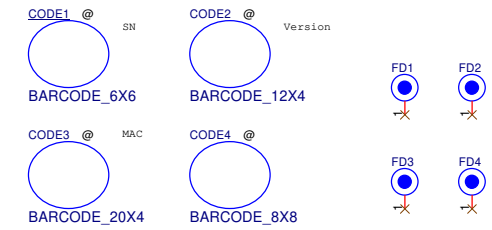


SSD

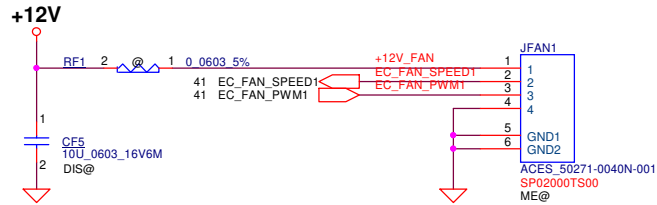


LASER BARCODE

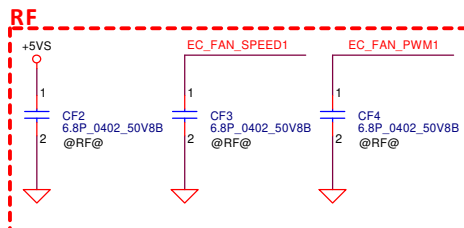
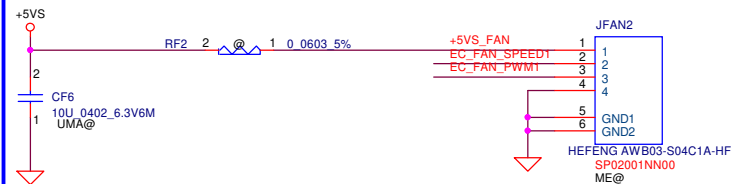
<https://vinafix.com>



+12V FAN

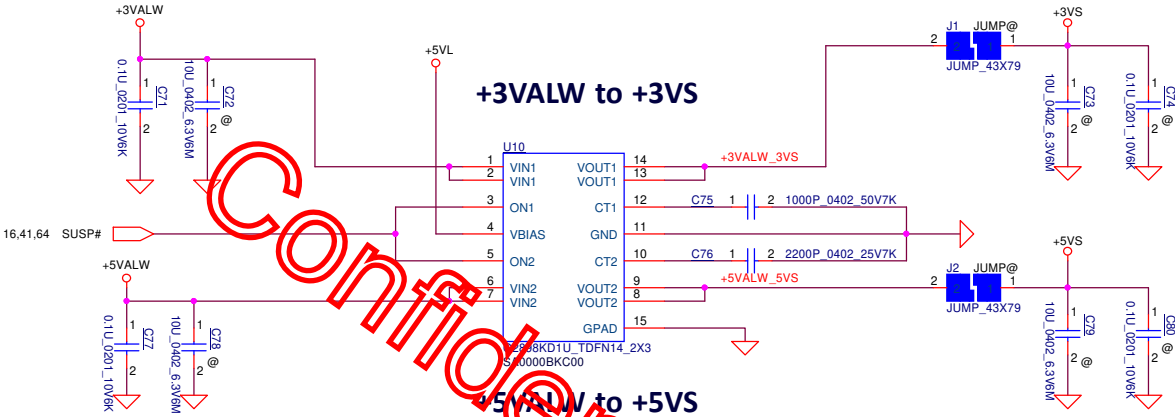


+5V FAN



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								Size		Document		Number		Rev	
								Custom				LA-LJ551PR02		0.2	
								Date:		Thursday, August 22, 2019		Sheet		46 of 67	

DC to DC



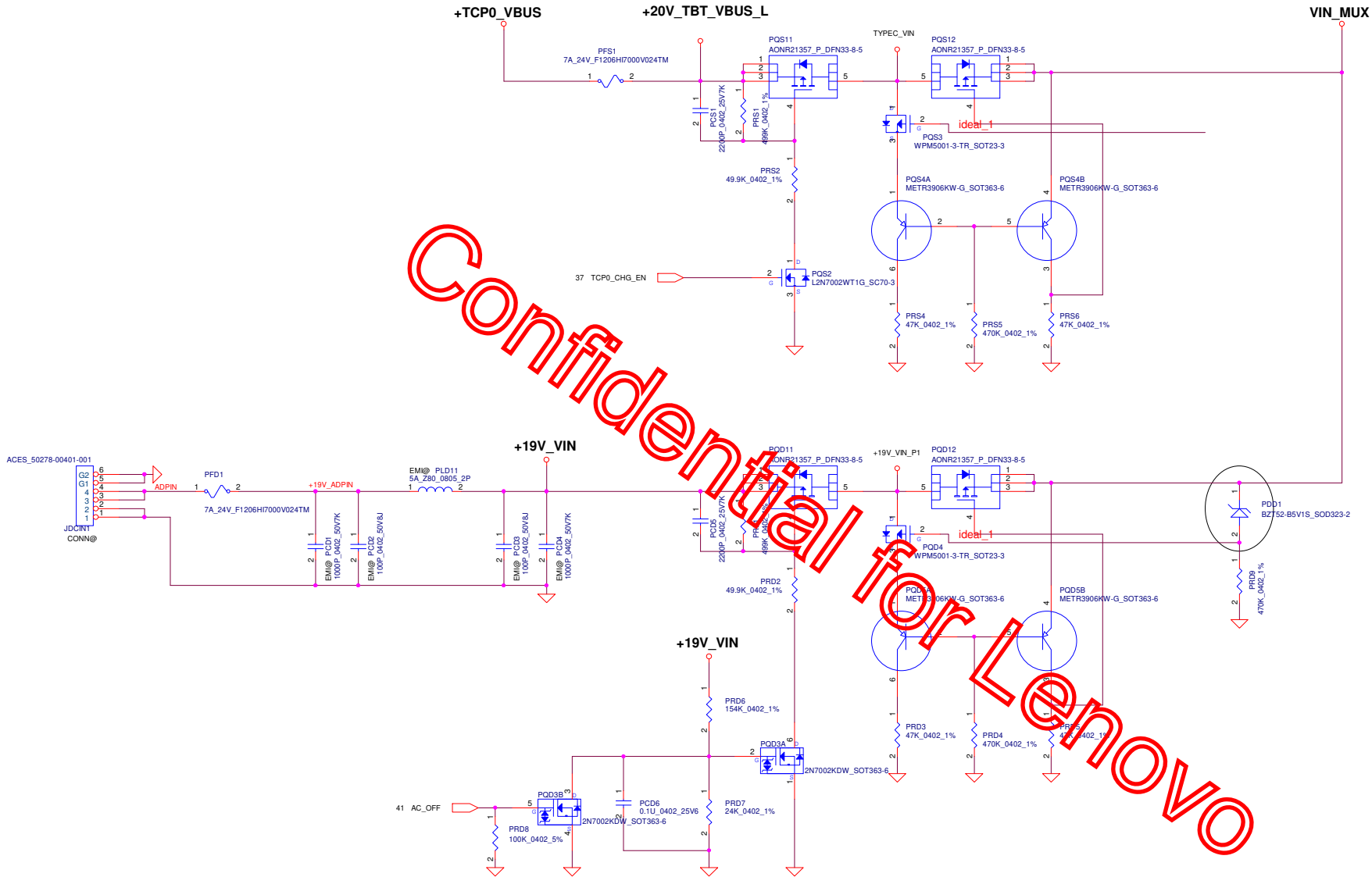
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Confidential for Lenovo

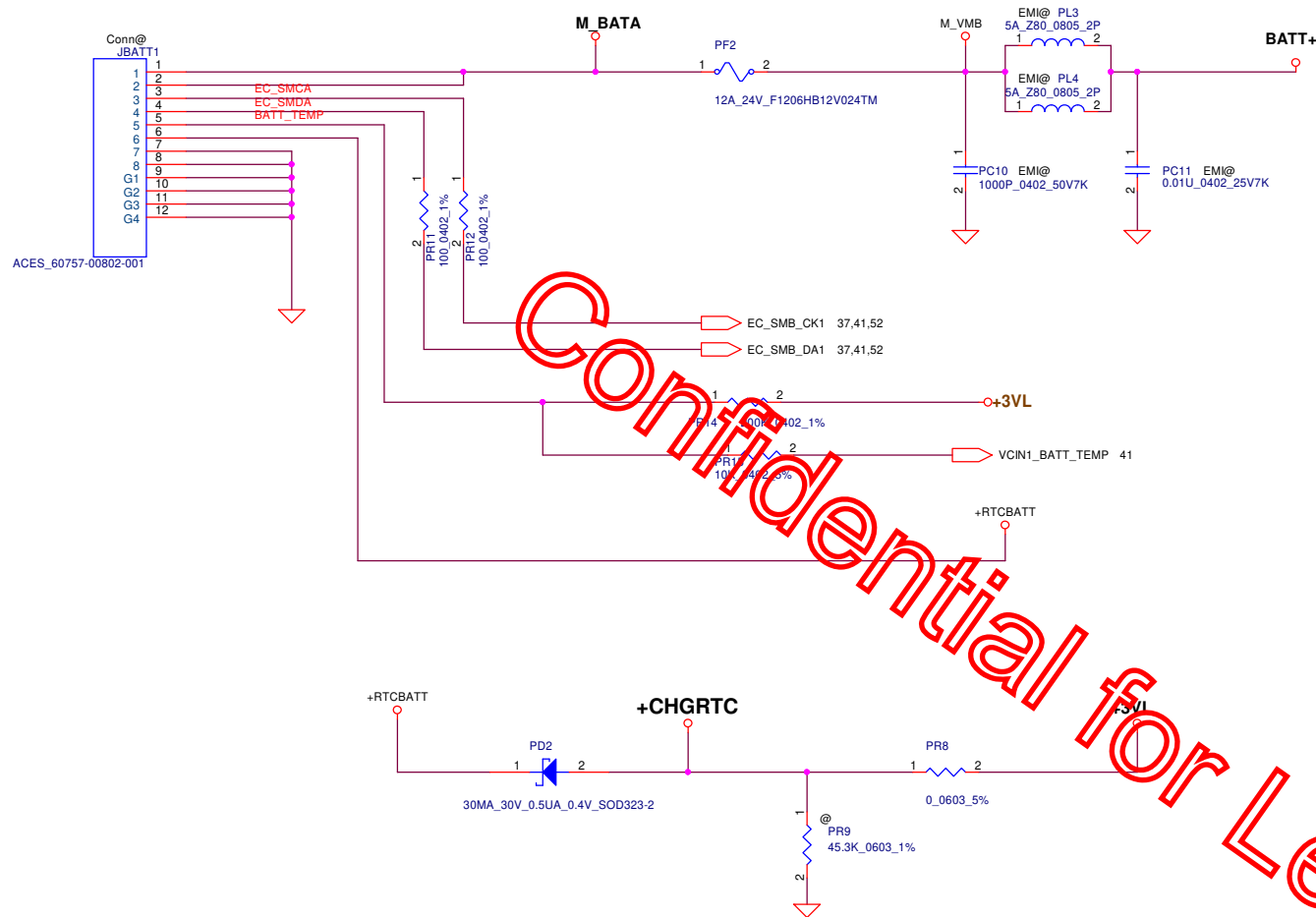
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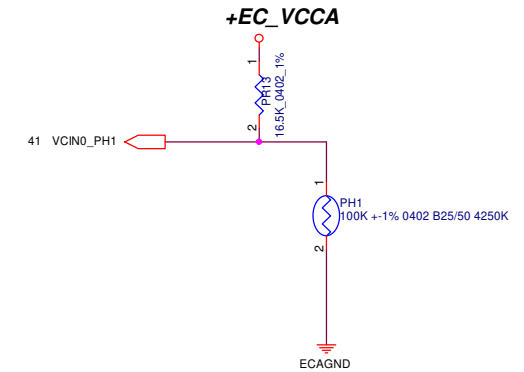
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				Size B	Rev 0.2
Date: Thursday, August 22, 2019		Sheet 49 of 67			



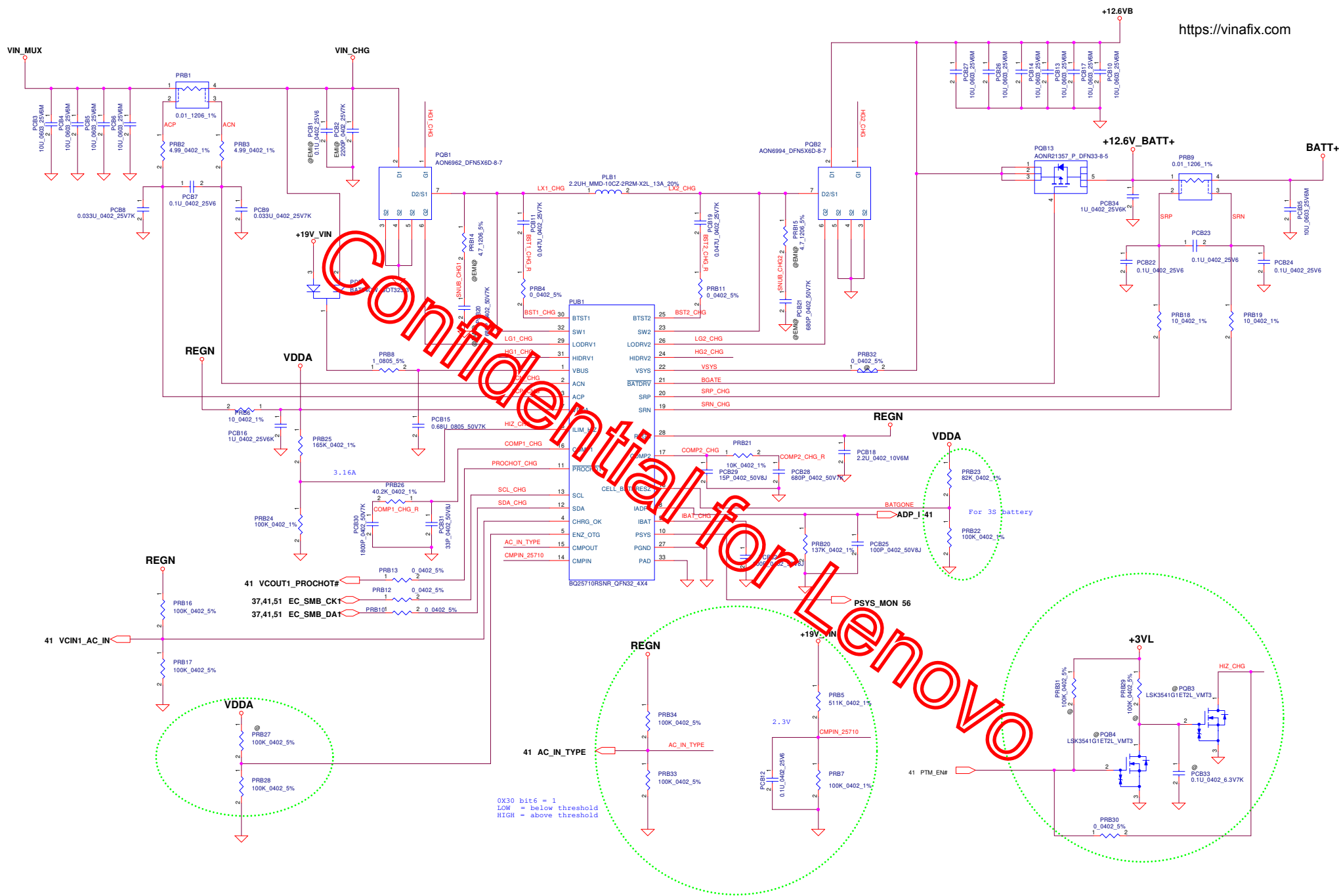
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Issued Date	2019/05/23	Deciphered Date	2021/05/31	Title	PWR- DC Conn/Type-C PD in
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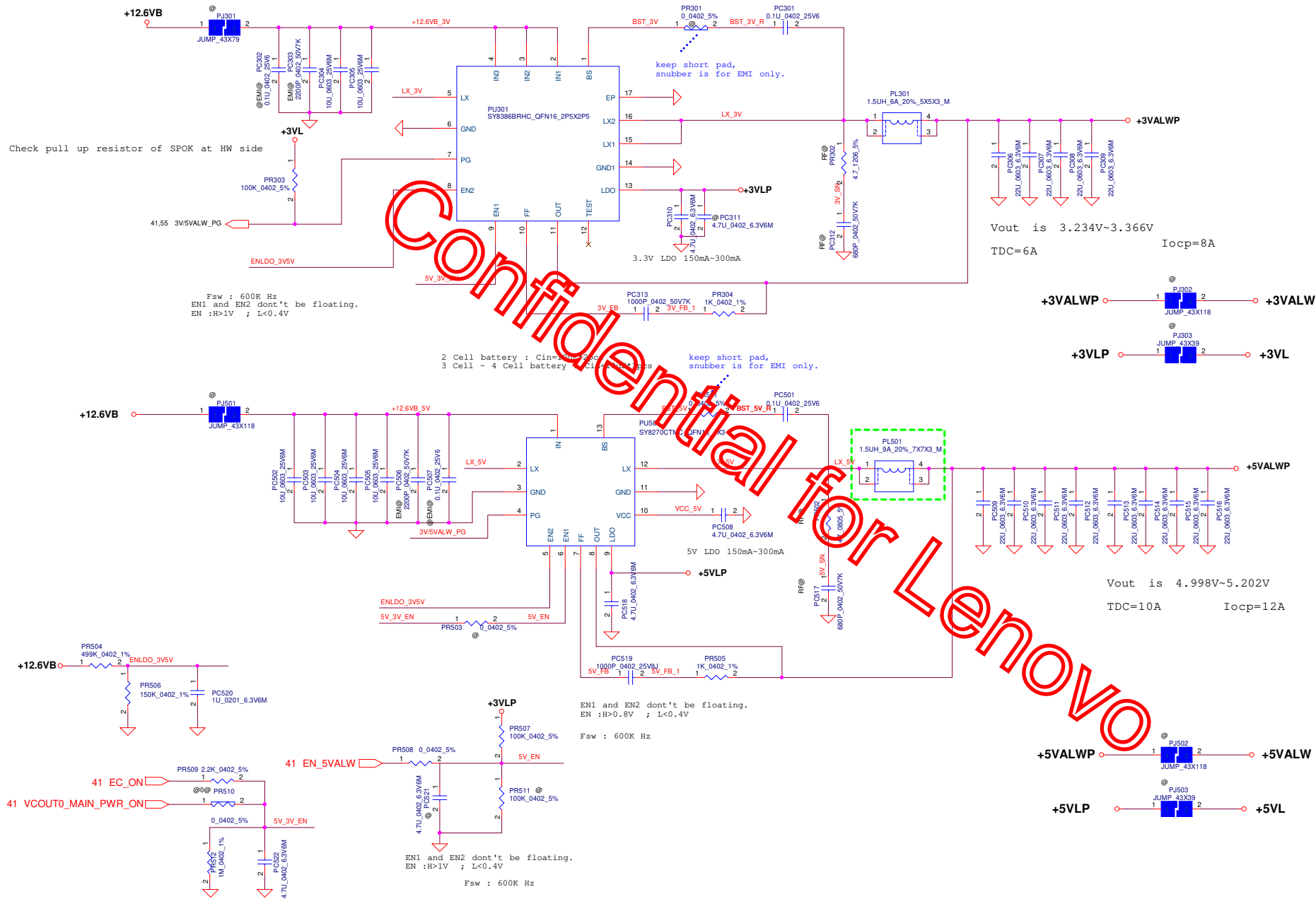
PH201 under CPU bottom side :
CPU thermal protection at 93 +3 degree C
Recovery at 56 +3 degree C



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Sheet	52 of 57

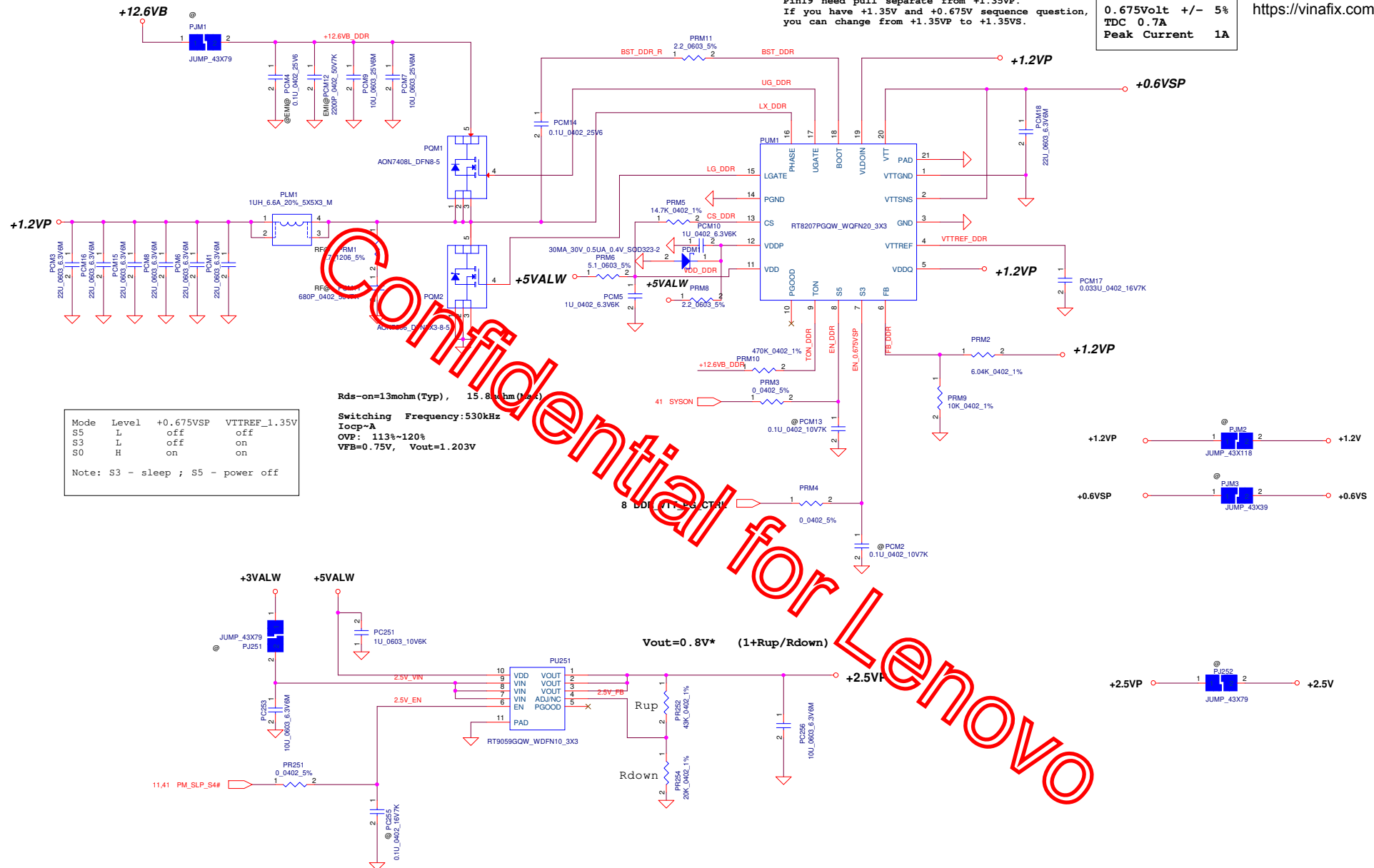


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Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

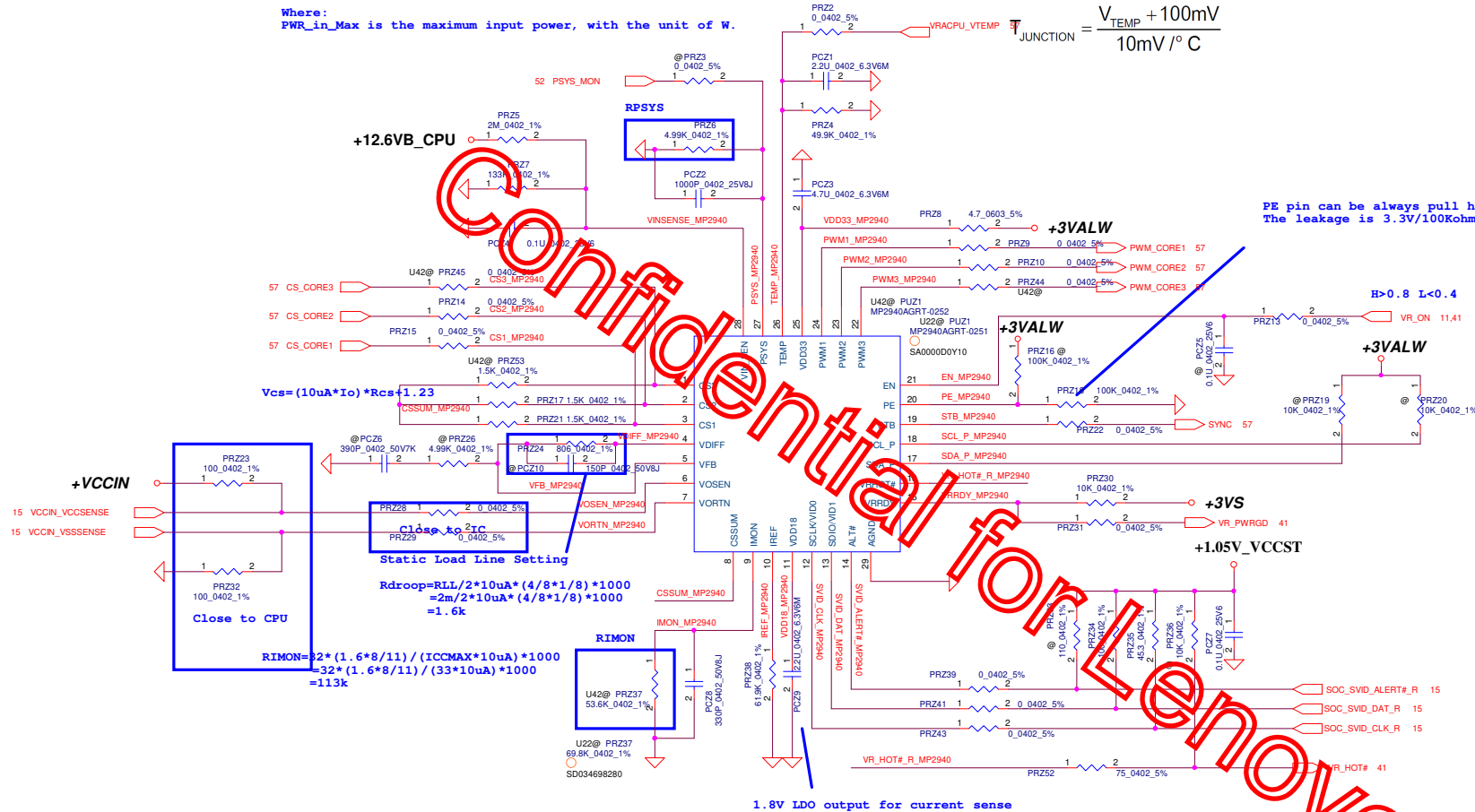
<https://vinafix.com>



Module model information <https://vinafix.com>
MP2940_V1A.mdd for IC portion
MP2940_V1B.mdd for SW portion

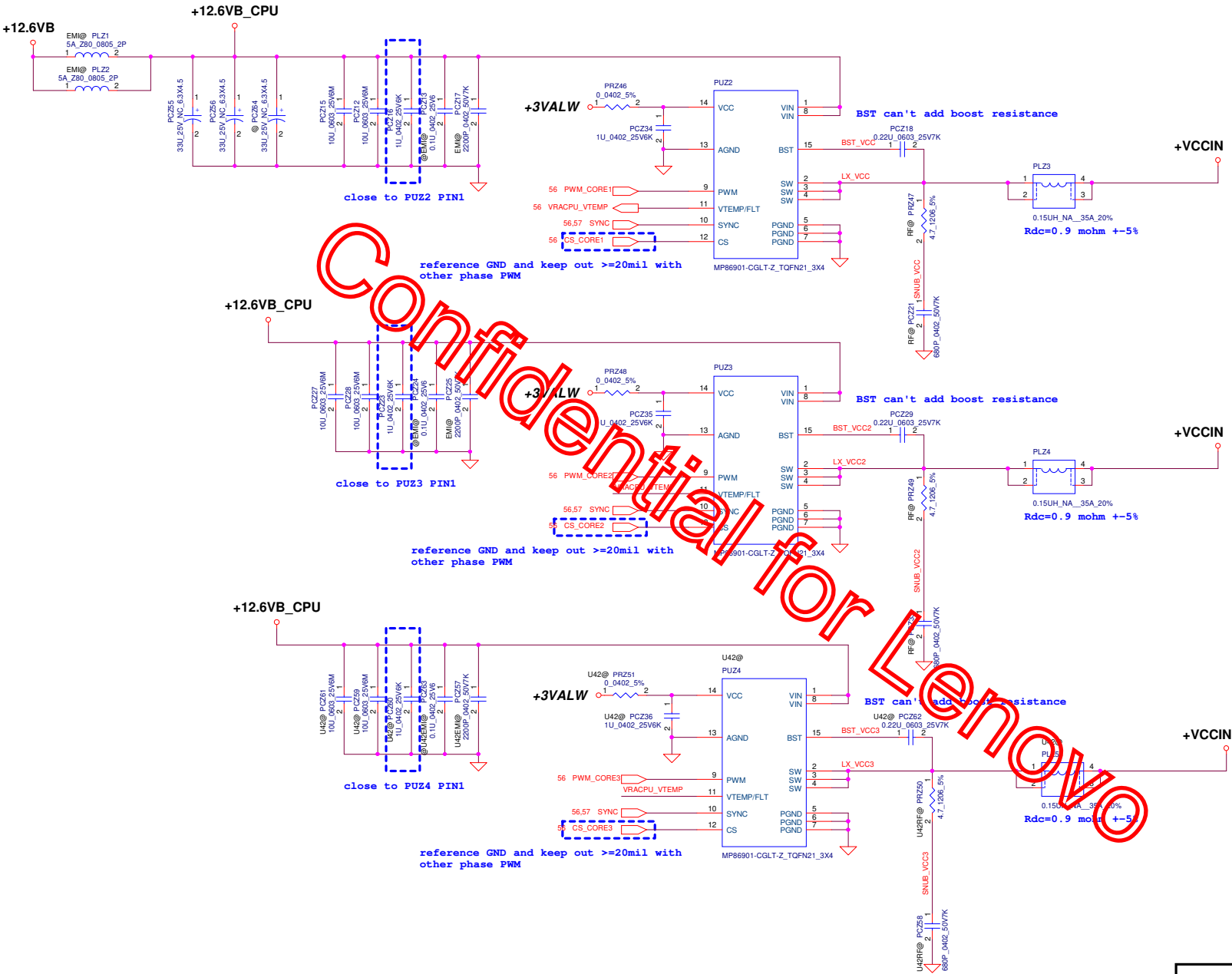
Rpsys=0.8/PWR_in_MAX*Isys
=0.8/160uA
=5k ohm

Where:
PWR_in_Max is the maximum input power, with the unit of W.



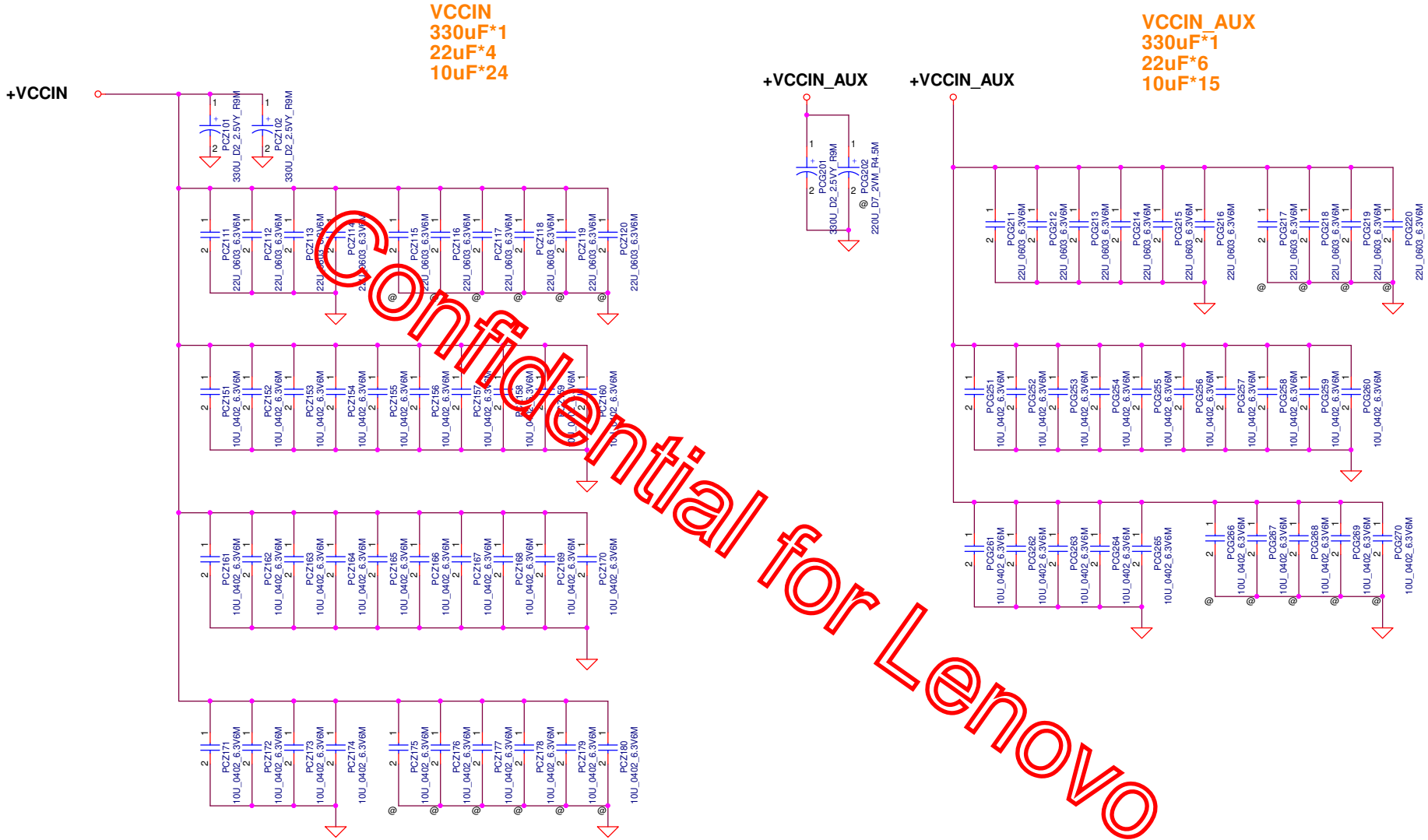
Function Field :
PWR.Plane.Regulator_MP2940:36.1
Rest of support elements:36.3

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Function Field :
Drivers:36.2
Rest of support elements:36.3
CPU_Core output CAP (Including MLCC):36.4

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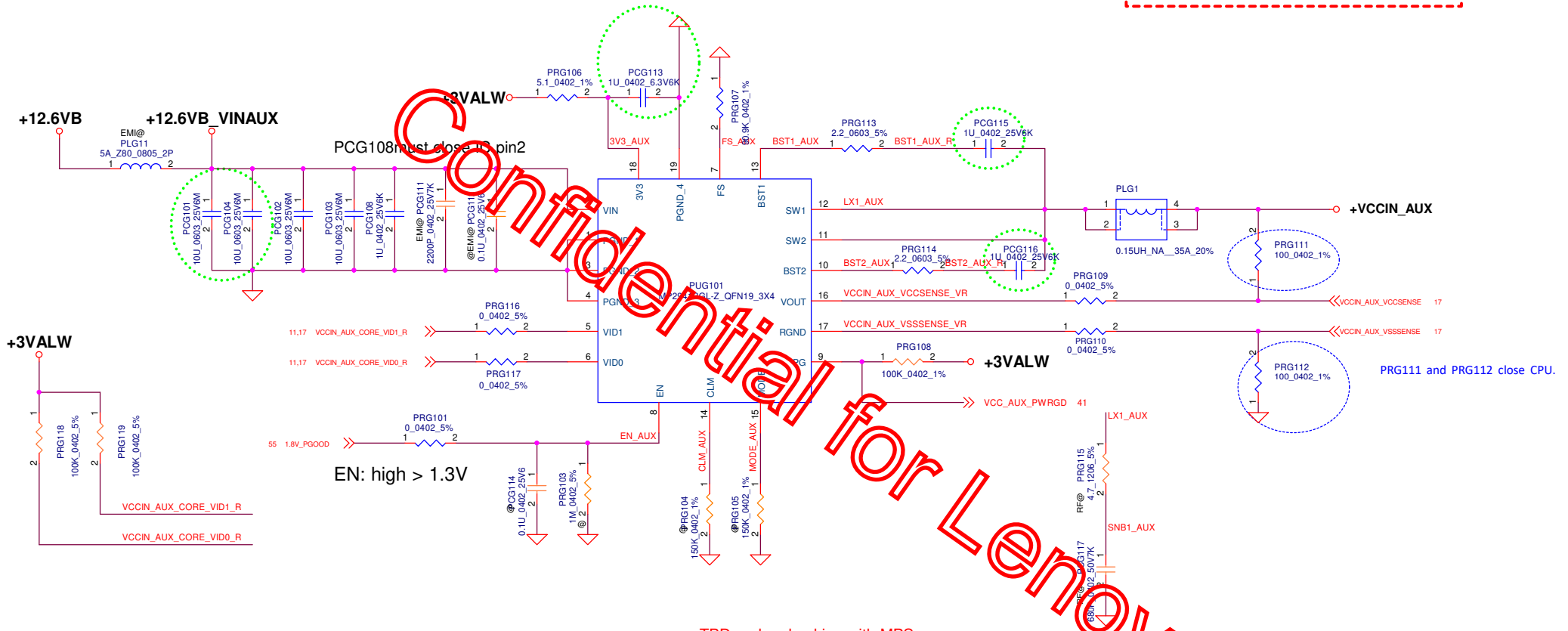
CPU PWR controller(36.1), Driver MOS(36.2), Support component(36.3)

Module model information
MP2941_V1.mdd

https://vinafix.com

VCCIN_AUX (Base on PDG rev 0.71)
Peak Current 26A (ICCmax)
TDC :10A
DC Load line :TBD mV/A
AC Load line :TBD mV/A
OCP Current 32A
Fsw=700kHz

ES need to change to SA0000BJK10



TBD under checking with MPS

Table---1:VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table---2:CLM Select

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	17A	>230k or float

Table---3:MODE Select

State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Table---4:FS Select

State	Fs(kHz)	Resistor to GND
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

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		Deciphered Date		PWR- VCCIN_AUX(MP2941)	
		2021/05/31		Size	
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R1, R2, R3, R4, R5, C are based on VGA type to set.

OpenVReg Configurations:(PSI pin)

Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.4V
1 phase with CCM	0.7V to 0.88V
2 phase with DEM	1.08V to 1.35V
2 phase with CCM	1.6V to 5.5V

PSI pull up on HW side

https://vinafix.com

$$V_{boot} = V_{vref} * R_{ref2} / (R_{ref1} + R_{ref2} + R_{boot})$$

$$R_t = R_{refadj} // (R_{boot} + R_{ref2})$$

$$V_{min} = V_{vref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R_t / (R_{ref1} + R_t)]$$

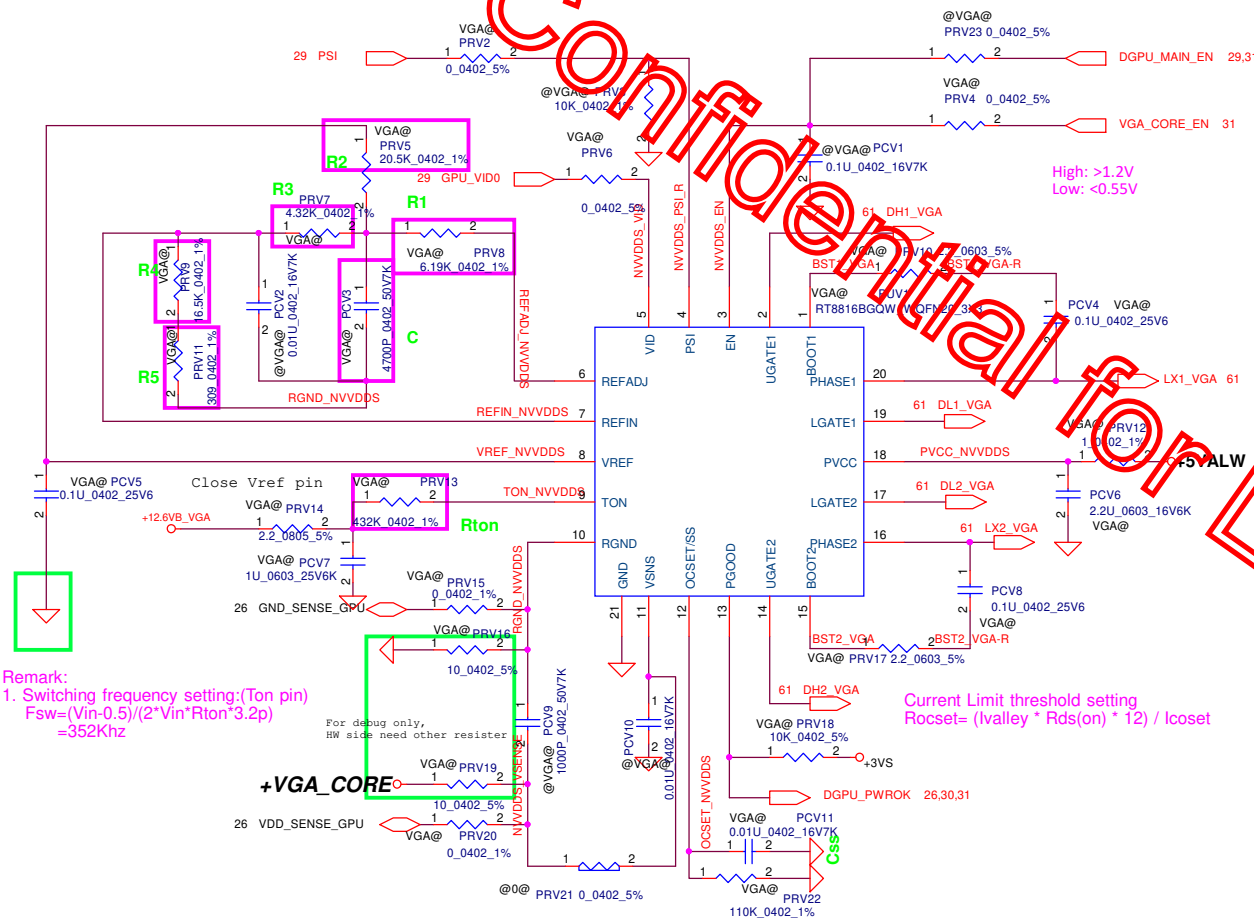
$$V_{max} = V_{vref} * R_{ref2} / [(R_{ref1} // R_{refadj}) + R_{boot} + R_{ref2}]$$

$$V_{out} = V_{min} + N * V_{step}$$

$$V_{step} = (V_{max} - V_{min}) / N_{max}$$

PWM VID and Output voltage control

- 1.Boot mode
- 2.Standby mode (don't support)
- 3.Normal mode



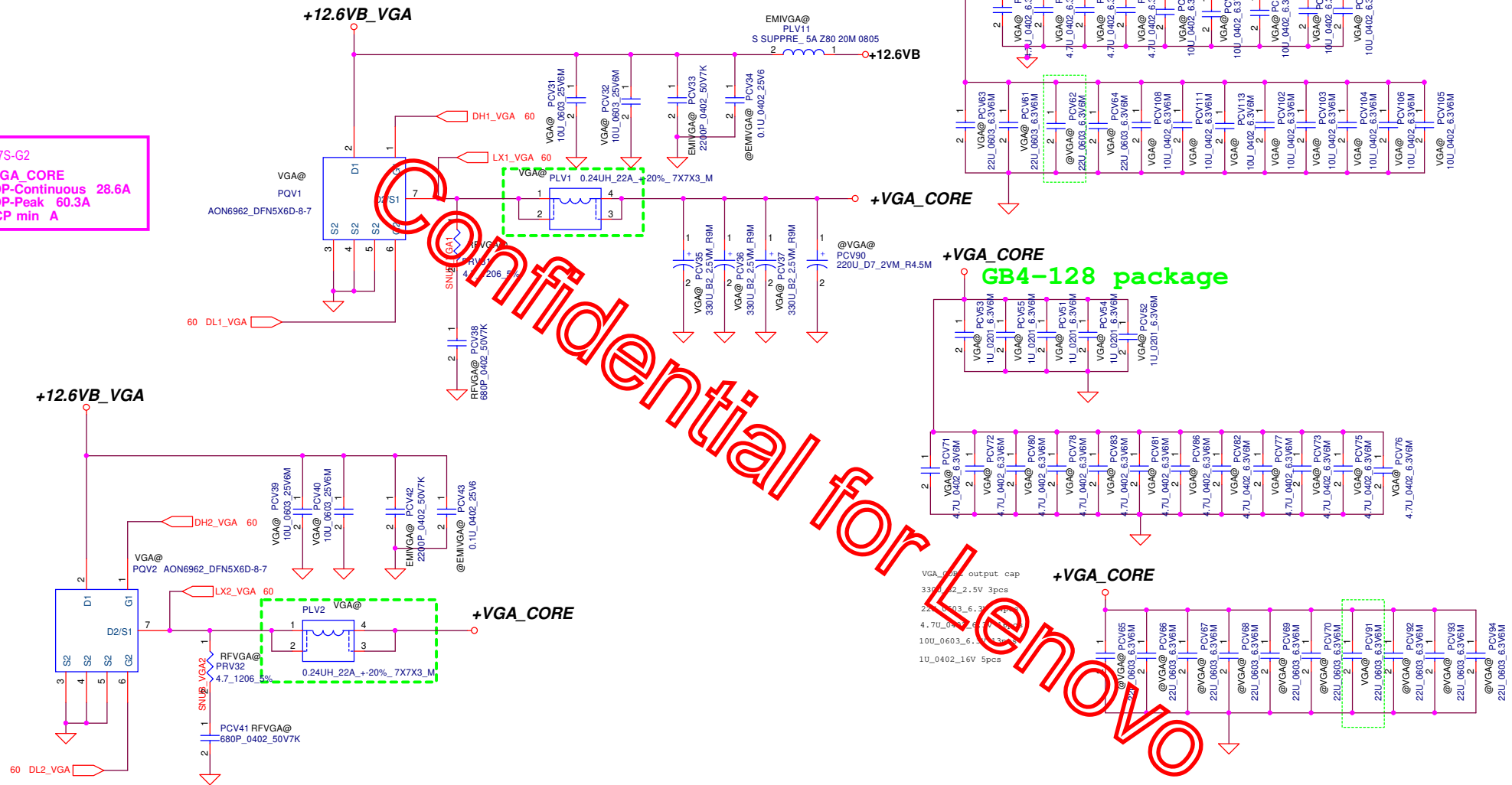
Remark:
1. Switching frequency setting:(Ton pin)
 $F_{sw} = (V_{in} - 0.5) / (2 * V_{in} * R_{ton} * 3.2p)$
 $= 352KHz$

Current Limit threshold setting
 $R_{ocset} = (I_{valley} * R_{ds(on)} * 12) / I_{coset}$

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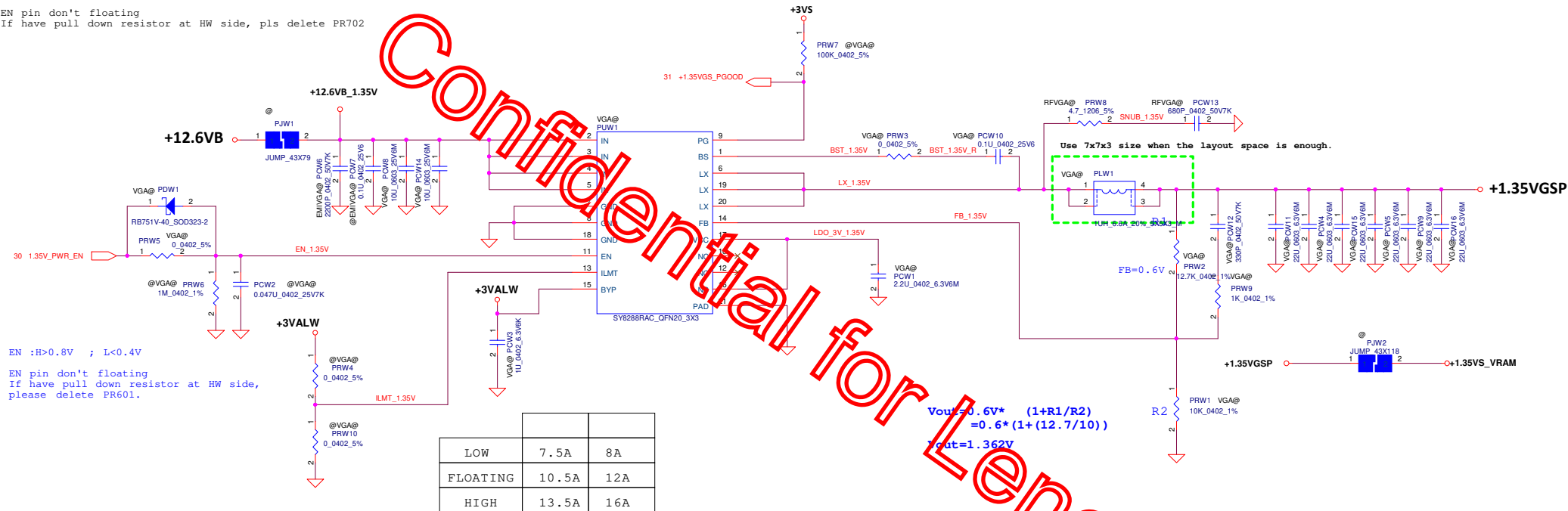
<https://vinafix.com>

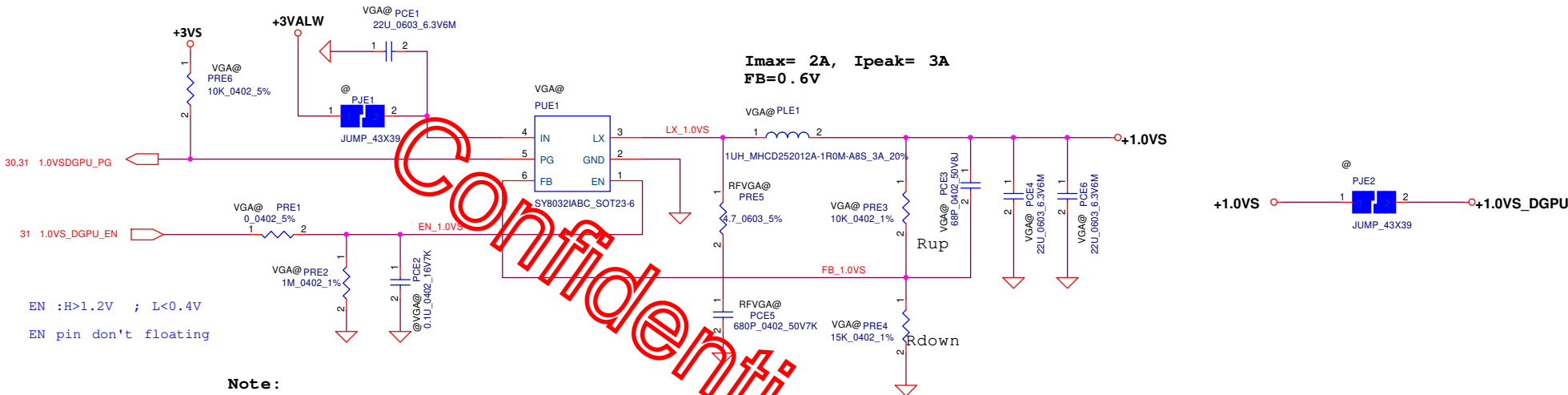
```
+VGA_CORE
EDP-Continuous 28.6A
EDP-Peak 60.3A
OCP min A
```



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EN pin don't floating
If have pull down resistor at HW side, pls delete PR702

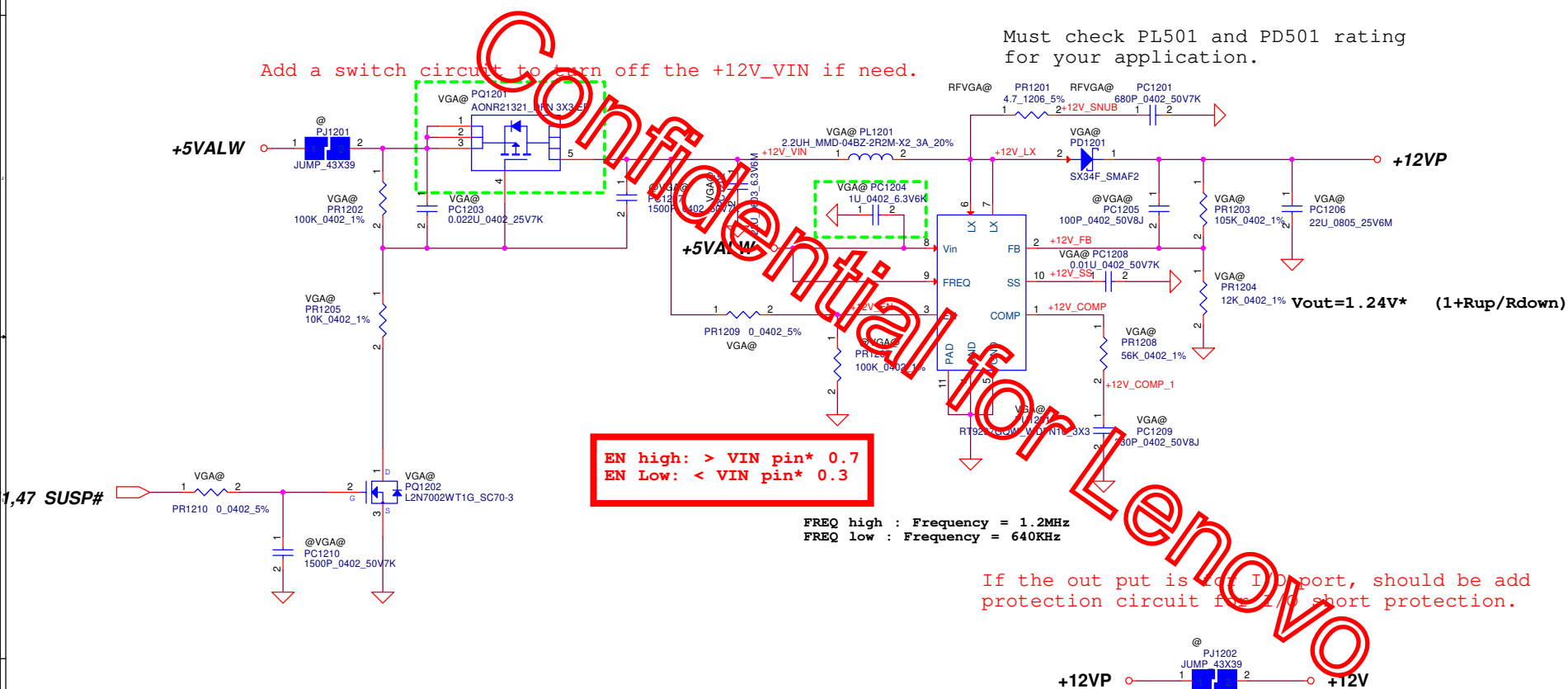




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Module model information

RT9297_V1.mdd



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Version change list
(P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
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